



# P67H2-A3

Rev : 1.0

ECS CONFIDENTIAL

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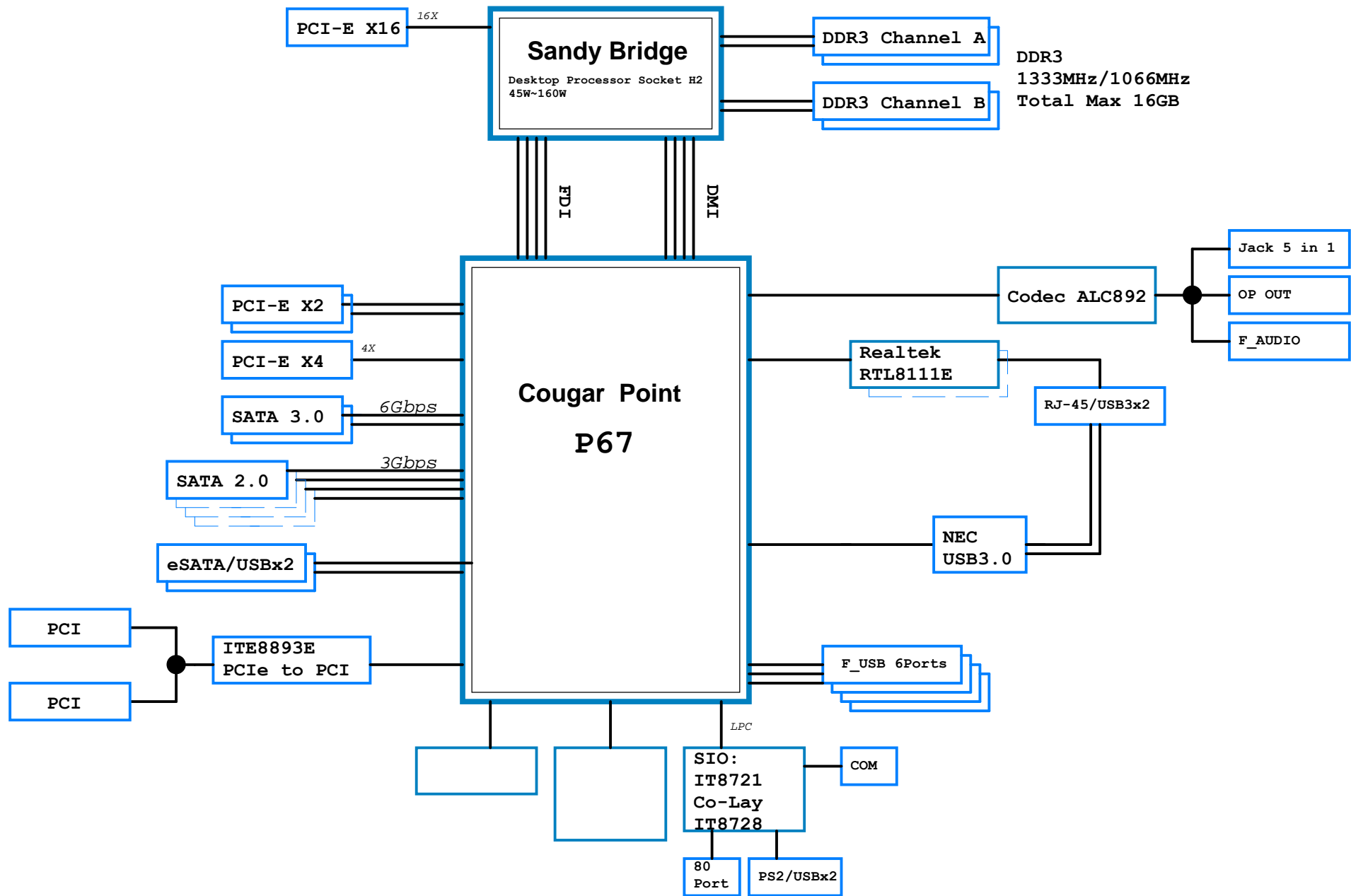
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NOTE:  
Design by 428971\_428971\_Sugar\_Bay\_and\_BromolowWS\_PDG\_Rev\_0\_8.pdf,  
428880\_428880\_Cougar\_Point\_Desktop\_Ballout\_Mech\_Package\_Rev1p0.zip

## REVISION HISTORY:

Rev	Date	Notes
V.A	2010/04/16	Initial version
V.B	2010/06/22	
V.1.0	2010/08/09	

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## 3PIO function

Pin Name	Power Well	Usage	Default Status
GPIO0	VCC3	FP_AUD_DETECT	GPI
GPIO1	VCC3	GP1_BOMDET2	GPI
GPIO6	VCC3	GP6_BOMDET3	GPI
GPIO7	VCC3	GP6_BOMDET4	GPI
GPIO9	3VSB	USB_OC_L5	Native
GPIO10	3VSB	USB_OC_L6	Native
GPIO11	3VSB	GP6_BOMDET4	Native
GPIO12	3VSB	GP6_BOMDET4	Native
GPIO13	3VSB	GP6_BOMDET4	GPI
GPIO14	3VSB	USB_OC_L7	Native
GPIO16	VCC3	Reserve for TPM	GPI
GPIO17	VCC3	GP17_BOMDET1	GPI
GPIO21	VCC3	GPIO21_COM2_DET	GPI
GPIO22	VCC3	CLR_CMOS_GP22	GPI
GPIO24	3VSB	PCH_SKTOCC_L	GPO
GPIO34	VCC3	GPIO34_TCM_PST_L	GPI
GPIO38	VCC3	GPIO38_TCM	GPI
GPIO39	VCC3	GPIO39_CASE0	GPI
GPIO40	3VSB	USB_OC_L1	Native
GPIO41	3VSB	USB_OC_L2	Native
GPIO42	3VSB	USB_OC_L3	Native
GPIO43	3VSB	USB_OC_L4	Native
GPIO48	VCC3	GPIO48_CASE1	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO59	3VSB	USB_OC_L0	Native
GPIO68	VCC3	GPIO68_USBDET1	GPI
GPIO69	VCC3	GPIO69_USBDET2	GPI
GPIO70	VCC3	GPIO70_USBDET3	Native
GPIO71	VCC3	Reserve for TPM	Native
GPIO72	3VSB	GPIO72_BOMDET5	Native

## SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16		SIO_BEEP	
GP23		Power LED	
GP22		Power LED	
GP52		FAN_TAC2	
GP51		FAN_CTL2	
GP37		FAN_TAC3	
GP36		FAN_CTL3	
GP30		8723_ATXPWRGD	
GP26		COM	
GP27		COM	
GP24		COM	
GP25		COM	
GP21		COM	
GP20		COM	
GP17		COM	
GP12		SIO_PCIRST1_L	
GP11		SIO_PCIRST2_L	
GP14		PWRGD1	
GP62		KBRST_L	
GP44		SIO_PWRBTN_L	
GP54		LPC_PME_L	
GP43		FP_PWRBTN_L	
GP42		SIO_PSON_L	
GP17		COM	
GP56		MCLK	
GP57		MDATA	
GP60		KCLK	
GP61		KDATA	
GP10		SIO_PCIRST3_L	
GP55		RSMRST_R_L	

## PCH Strap Pin

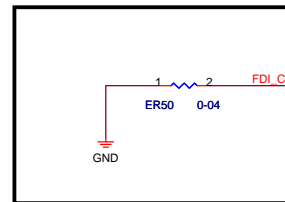
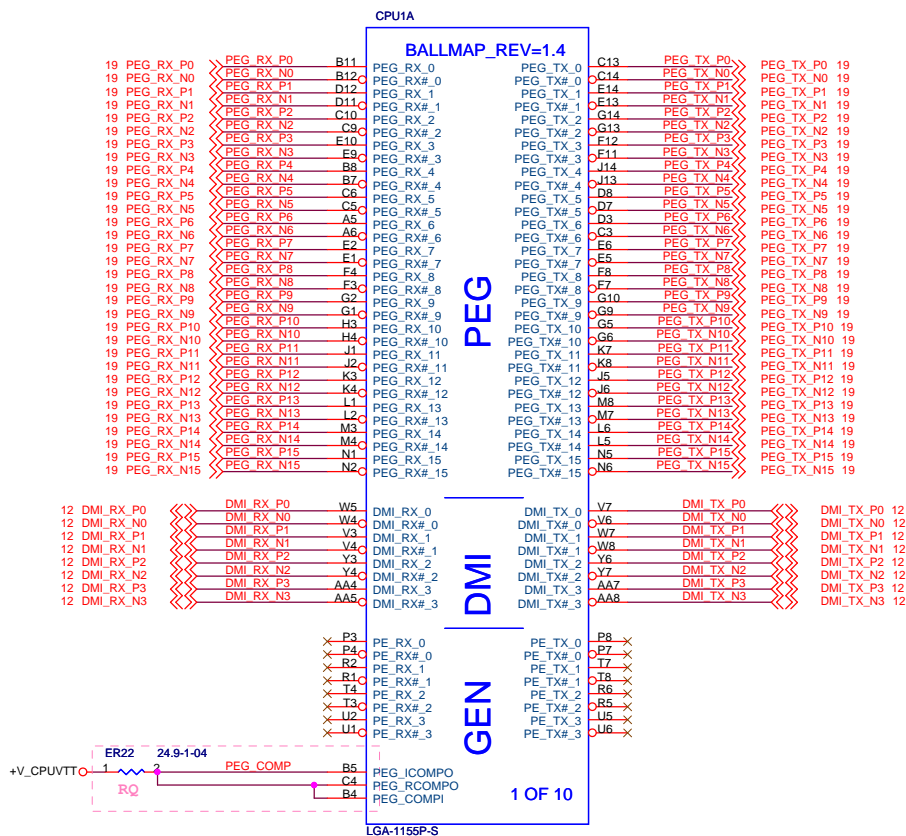
Pin Name	Usage	Default Status
SPKR	No Reboot	20K internal pull-down · No Reboot Mode with TCO Disabled:
INIT3_3V#	Reserved	20K internal pull-up · intend for Firmware Hub.
GNT[3]#/GPIO[55]	Disable Top-Block Swap	20K internal pull-up · "topblock swap" mode Disable
INTVRMEN	Enable Integrated 1.05V VRM	Need External Pull-up · Integrated 1.05V VRM Enable
GNT1# / GPIO51	Boot BIOS Strap bit [1] BBS[1]	20K internal pull-up · The default flash selection is the SPI flash.All
SATA1GP / GPIO19	Boot BIOS Strap bit[0] BBS[0]	20K internal pull-up · The default flash selection is the SPI flash.All
HDA_SDO	Flash Descriptor Security Override/ ME	Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default)
DF_TV5	Enable DMI termination voltage	This signal has a weak internal pull-down.
GPIO28	Eable On-Die PLL Voltage Regulator	The On-Die PLL voltage regulator is enabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select 1.8V	20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	Enable TLS Confidentiality	Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.

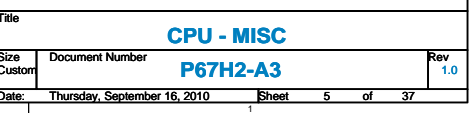
Table 7-1. Power On Strapping Options

	Symbol	Strapping Event	Value	Description
JP2 Pin 122	Flashseg1_EN	Internal VCC-OK/LRESET#	1	Disable
			0	Enable Flash I/F Address Segment FFF8_0000 ~ FFFF_FFFF & 000E_0000 ~ 000F_FFFF
JP4 Pin 126	K8PWR_EN	Internal VCC-OK	1	Disable K8 power sequence function
			0	Enable K8 power sequence function
JP3,JP5 Pin 124 & Pin 46	FAN_CTL_SE L	Internal VCC-OK	11	The default value of EC Index 63h/6Bh/73h is 80h.
			10	The default value of EC Index 63h/6Bh/73h is FFh.
			01	The default value of EC Index 63h/6Bh/73h is 00h.
			00	The default value of EC Index 63h/6Bh/73h is 40h.

## Elitegroup Computer Systems

Title <b>30-GPIO Function Map</b>			
Size Custom	Document Number <b>P67H2-A3</b>		Rev <b>1.0</b>
Date:	Monday, August 30, 2010	Sheet	3 of 37





9 M_DATA_A[0..63]	← M_DATA A[0..63]
9 M_DQS_A_P[0..7]	← M_DQS A P[0..7]
9 M_DQS_A_N[0..7]	← M_DQS A N[0..7]
9 M_MA_A[0..15]	← M_MA A[0..15]
9 M_BS_A[0..2]	← M_BS A[0..2]
9 M_CS_A_L[0..3]	← M_CS A L[0..3]
9 M_CKE_A[0..3]	← M_CKE A[0..3]
9 M_ODT_A[0..3]	← M_ODT A[0..3]
9 M_CLK_A_P[0..3]	← M_CLK A P[0..3]
9 M_CLK_A_N[0..3]	← M_CLK A N[0..3]
9 M_WE_A_L	← M_WE A L
9 M_CAS_A_L	← M_CAS A L
9 M_RAS_A_L	← M_RAS A L

DDR3 CH.A

9,10 DDR3\_DRAMRST\_L ← DDR3\_DRAMRST\_L

10 M_DATA_B[0..63]	← M_DATA B[0..63]
10 M_DQS_B_P[0..7]	← M_DQS B P[0..7]
10 M_DQS_B_N[0..7]	← M_DQS B N[0..7]
10 M_MA_B[0..15]	← M_MA B[0..15]
10 M_BS_B[0..2]	← M_BS B[0..2]
10 M_CS_B_L[0..3]	← M_CS B L[0..3]
10 M_CKE_B[0..3]	← M_CKE B[0..3]
10 M_ODT_B[0..3]	← M_ODT B[0..3]
10 M_CLK_B_P[0..3]	← M_CLK B P[0..3]
10 M_CLK_B_N[0..3]	← M_CLK B N[0..3]
10 M_WE_B_L	← M_WE B L
10 M_CAS_B_L	← M_CAS B L
10 M_RAS_B_L	← M_RAS B L

DDR3 CH.B

M_DATA_A0	AJ3	SA_DQ_0
M_DATA_A1	AJ4	SA_DQ_1
M_DATA_A2	AL3	SA_DQ_2
M_DATA_A3	AL4	SA_DQ_3
M_DATA_A4	AJ2	SA_MA_4
M_DATA_A5	AJ1	SA_MA_5
M_DATA_A6	AL1	SA_MA_6
M_DATA_A7	AL2	SA_MA_7
M_DATA_A8	AN1	SA_MA_8
M_DATA_A9	AN4	SA_MA_9
M_DATA_A10	AR3	SA_MA_10
M_DATA_A11	AR4	SA_MA_11
M_DATA_A12	AN2	SA_MA_12
M_DATA_A13	AR2	SA_MA_13
M_DATA_A14	AR1	SA_MA_14
M_DATA_A15	AV2	SA_MA_15
M_DATA_A16	AV3	SA_MA_16
M_DATA_A17	AV5	SA_MA_17
M_DATA_A18	AU3	SA_MA_18
M_DATA_A19	AU2	SA_MA_19
M_DATA_A20	AU1	SA_MA_20
M_DATA_A21	AU3	SA_MA_21
M_DATA_A22	AU5	SA_MA_22
M_DATA_A23	AV5	SA_MA_23
M_DATA_A24	AV7	SA_MA_24
M_DATA_A25	AU7	SA_MA_25
M_DATA_A26	AV9	SA_MA_26
M_DATA_A27	AU9	SA_MA_27
M_DATA_A28	AV7	SA_MA_28
M_DATA_A29	AV7	SA_MA_29
M_DATA_A30	AU7	SA_MA_30
M_DATA_A31	AY9	SA_MA_31
M_DATA_A32	AU35	SA_MA_32
M_DATA_A33	AW37	SA_MA_33
M_DATA_A34	AU39	SA_MA_34
M_DATA_A35	AW35	SA_MA_35
M_DATA_A36	AW35	SA_MA_36
M_DATA_A37	AY36	SA_MA_37
M_DATA_A38	AU38	SA_MA_38
M_DATA_A39	AU37	SA_MA_39
M_DATA_A40	AR37	SA_MA_40
M_DATA_A41	AR37	SA_MA_41
M_DATA_A42	AN35	SA_MA_42
M_DATA_A43	AN37	SA_MA_43
M_DATA_A44	AR39	SA_MA_44
M_DATA_A45	AR38	SA_MA_45
M_DATA_A46	AN39	SA_MA_46
M_DATA_A47	AN40	SA_MA_47
M_DATA_A48	AL40	SA_MA_48
M_DATA_A49	AL37	SA_MA_49
M_DATA_A50	AJ38	SA_MA_50
M_DATA_A51	AJ37	SA_MA_51
M_DATA_A52	AL38	SA_MA_52
M_DATA_A53	AL38	SA_MA_53
M_DATA_A54	AJ39	SA_MA_54
M_DATA_A55	AJ40	SA_MA_55
M_DATA_A56	AG40	SA_MA_56
M_DATA_A57	AG37	SA_MA_57
M_DATA_A58	AE38	SA_MA_58
M_DATA_A59	AE37	SA_MA_59
M_DATA_A60	AG39	SA_MA_60
M_DATA_A61	AG38	SA_MA_61
M_DATA_A62	AE39	SA_MA_62
M_DATA_A63	AE40	SA_MA_63

M_DQS_A_P0	AK3	SA_DQS_0
M_DQS_A_P1	AP3	SA_DQS_1
M_DQS_A_P2	AW4	SA_DQS_2
M_DQS_A_P3	AV8	SA_DQS_3
M_DQS_A_P4	AV37	SA_DQS_4
M_DQS_A_P5	AP38	SA_DQS_5
M_DQS_A_P6	AK38	SA_DQS_6
M_DQS_A_P7	AF38	SA_DQS_7

M_DQS_A_N0	AK2	SA_DQS#_0
M_DQS_A_N1	AP2	SA_DQS#_1
M_DQS_A_N2	AV4	SA_DQS#_2
M_DQS_A_N3	AW8	SA_DQS#_3
M_DQS_A_N4	AV38	SA_DQS#_4
M_DQS_A_N5	AP39	SA_DQS#_5
M_DQS_A_N6	AK39	SA_DQS#_6
M_DQS_A_N7	AF39	SA_DQS#_7

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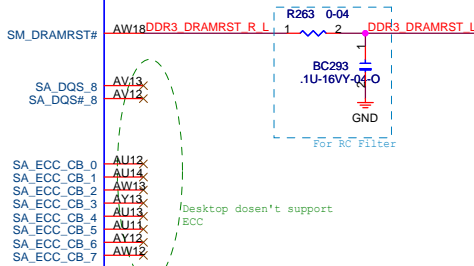
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SA\_DQS#\_8

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SA\_ECC\_CB\_2  
SA\_ECC\_CB\_3  
SA\_ECC\_CB\_4  
SA\_ECC\_CB\_5  
SA\_ECC\_CB\_6  
SA\_ECC\_CB\_7

DDR\_0  
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LGA-1155P-S

DDR3 CH.A



Pay Attention to This Part!

M_DATA_B0	AG7	SB_DQ_0
M_DATA_B1	AG8	SB_DQ_1
M_DATA_B2	AJ8	SB_DQ_2
M_DATA_B3	AG5	SB_DQ_3
M_DATA_B4	AG6	SB_DQ_4
M_DATA_B5	AJ6	SB_DQ_5
M_DATA_B6	AJ7	SB_DQ_6
M_DATA_B7	AL7	SB_DQ_7
M_DATA_B8	AM7	SB_DQ_8
M_DATA_B9	AM7	SB_DQ_9
M_DATA_B10	AM10	SB_DQ_10
M_DATA_B11	AL10	SB_DQ_11
M_DATA_B12	AL6	SB_DQ_12
M_DATA_B13	AL9	SB_DQ_13
M_DATA_B14	AM9	SB_DQ_14
M_DATA_B15	AP7	SB_DQ_15
M_DATA_B16	AR7	SB_DQ_16
M_DATA_B17	AP10	SB_DQ_17
M_DATA_B18	AR10	SB_DQ_18
M_DATA_B19	AP6	SB_DQ_19
M_DATA_B20	AR6	SB_DQ_20
M_DATA_B21	AP9	SB_DQ_21
M_DATA_B22	AR9	SB_DQ_22
M_DATA_B23	AM12	SB_DQ_23
M_DATA_B24	AM13	SB_DQ_24
M_DATA_B25	AP13	SB_DQ_25
M_DATA_B26	AP13	SB_DQ_26
M_DATA_B27	AL12	SB_DQ_27
M_DATA_B28	AL13	SB_DQ_28
M_DATA_B29	AP12	SB_DQ_29
M_DATA_B30	AP12	SB_DQ_30
M_DATA_B31	AR28	SB_DQ_31
M_DATA_B32	AR29	SB_DQ_32
M_DATA_B33	AL28	SB_DQ_33
M_DATA_B34	AL29	SB_DQ_34
M_DATA_B35	AP28	SB_DQ_35
M_DATA_B36	AP29	SB_DQ_36
M_DATA_B37	AM28	SB_DQ_37
M_DATA_B38	AM29	SB_DQ_38
M_DATA_B39	AP32	SB_DQ_39
M_DATA_B40	AP31	SB_DQ_40
M_DATA_B41	AP35	SB_DQ_41
M_DATA_B42	AP34	SB_DQ_42
M_DATA_B43	AR32	SB_DQ_43
M_DATA_B44	AR31	SB_DQ_44
M_DATA_B45	AR35	SB_DQ_45
M_DATA_B46	AR34	SB_DQ_46
M_DATA_B47	AM32	SB_DQ_47
M_DATA_B48	AM31	SB_DQ_48
M_DATA_B49	AL35	SB_DQ_49
M_DATA_B50	AL32	SB_DQ_50
M_DATA_B51	AM34	SB_DQ_51
M_DATA_B52	AL31	SB_DQ_52
M_DATA_B53	AM35	SB_DQ_53
M_DATA_B54	AL34	SB_DQ_54
M_DATA_B55	AH35	SB_DQ_55
M_DATA_B56	AH34	SB_DQ_56
M_DATA_B57	AE34	SB_DQ_57
M_DATA_B58	AE35	SB_DQ_58
M_DATA_B59	AJ35	SB_DQ_59
M_DATA_B60	AJ34	SB_DQ_60
M_DATA_B61	AF33	SB_DQ_61
M_DATA_B62	AF33	SB_DQ_62
M_DATA_B63	AF35	SB_DQ_63

M_DQS_B_P0	AH7	SB_DQS_0
M_DQS_B_P1	AM8	SB_DQS_1
M_DQS_B_P2	AR8	SB_DQS_2
M_DQS_B_P3	AN9	SB_DQS_3
M_DQS_B_P4	AP33	SB_DQS_4
M_DQS_B_P5	AL33	SB_DQS_5
M_DQS_B_P6	AG35	SB_DQS_6
M_DQS_B_P7	AG35	SB_DQS_7

M_DQS_B_N0	AH6	SB_DQS#_0
M_DQS_B_N1	AL8	SB_DQS#_1
M_DQS_B_N2	AP8	SB_DQS#_2
M_DQS_B_N3	AN12	SB_DQS#_3
M_DQS_B_N4	AN28	SB_DQS#_4
M_DQS_B_N5	AR33	SB_DQS#_5
M_DQS_B_N6	AM33	SB_DQS#_6
M_DQS_B_N7	AG34	SB_DQS#_7

CPU10

BALLMAP\_REV=1.4

SB_MA_0	AK24	M_MA_B0
SB_MA_1	AM20	M_MA_B1
SB_MA_2	AM19	M_MA_B2
SB_MA_3	AK18	M_MA_B3
SB_MA_4	AP19	M_MA_B4
SB_MA_5	AP18	M_MA_B5
SB_MA_6	AM18	M_MA_B6
SB_MA_7	AL18	M_MA_B7
SB_MA_8	AN18	M_MA_B8
SB_MA_9	AY17	M_MA_B9
SB_MA_10	AN23	M_MA_B10
SB_MA_11	AU17	M_MA_B11
SB_MA_12	AT18	M_MA_B12
SB_MA_13	AR26	M_MA_B13
SB_MA_14	AY16	M_MA_B14
SB_MA_15	AV16	M_MA_B15
SA_CK[2]	AR25	M_WE_B_L
SA_CK[1]	AK25	M_CAS_B_L
SA_ODT[2]	AP24	M_RAS_B_L
SB_BS_0	AP23	M_BS_B0
SB_BS_1	AM24	M_BS_B1
SB_BS_2	AW17	M_BS_B2
SB_CS#_0	AN25	M_CS_B_L0
SB_CS#_1	AN26	M_CS_B_L1
SB_CS#_2	AN25	M_CS_B_L2
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SB_CKE_0	AU16	M_CKE_B0
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SB_CKE_2	AV15	M_CKE_B3
SB_CKE_3		
SB_ODT_0	AL26	M_ODT_B0
SB_ODT_1	AP26	M_ODT_B2
SB_ODT_2	AK26	M_ODT_B3
SB_ODT_3		
SB_CK_0	AL21	M_CLK_B_P0
SB_CK#_0	AL22	M_CLK_B_N0
SB_CK_1	AL20	M_CLK_B_P1
SB_CK#_1	AK20	M_CLK_B_N1
SB_CK_2	AL23	M_CLK_B_P2
SB_CK#_2	AM22	M_CLK_B_N2
SB_CK_3	AP21	M_CLK_B_P3
SB_CK#_3	AN21	M_CLK_B_N3

SB\_DQS\_8  
SB\_DQS#\_8

SB\_ECC\_CB\_0  
SB\_ECC\_CB\_1  
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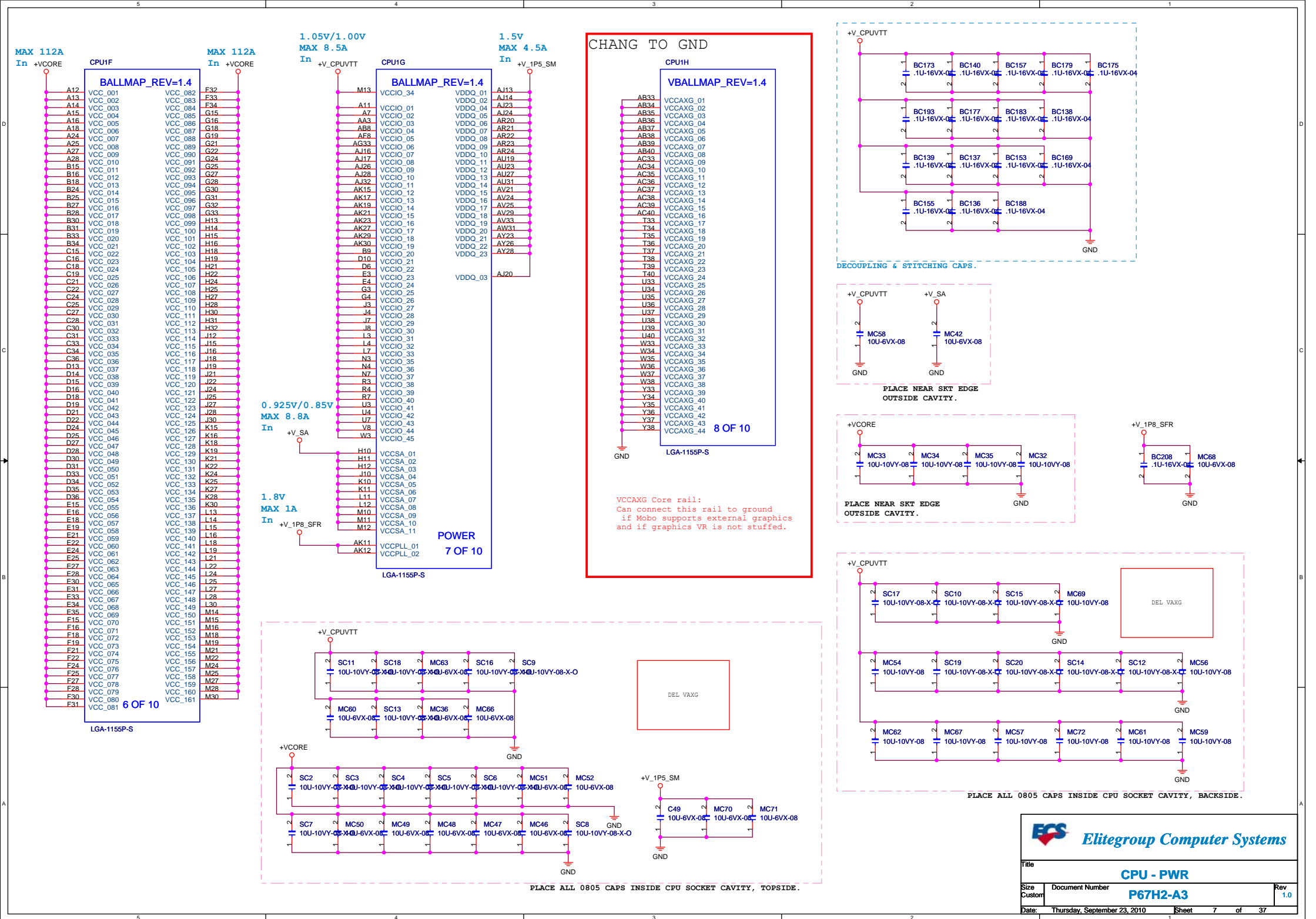
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LGA-1155P-S

DDR3 CH.B



Elitegroup Computer Systems

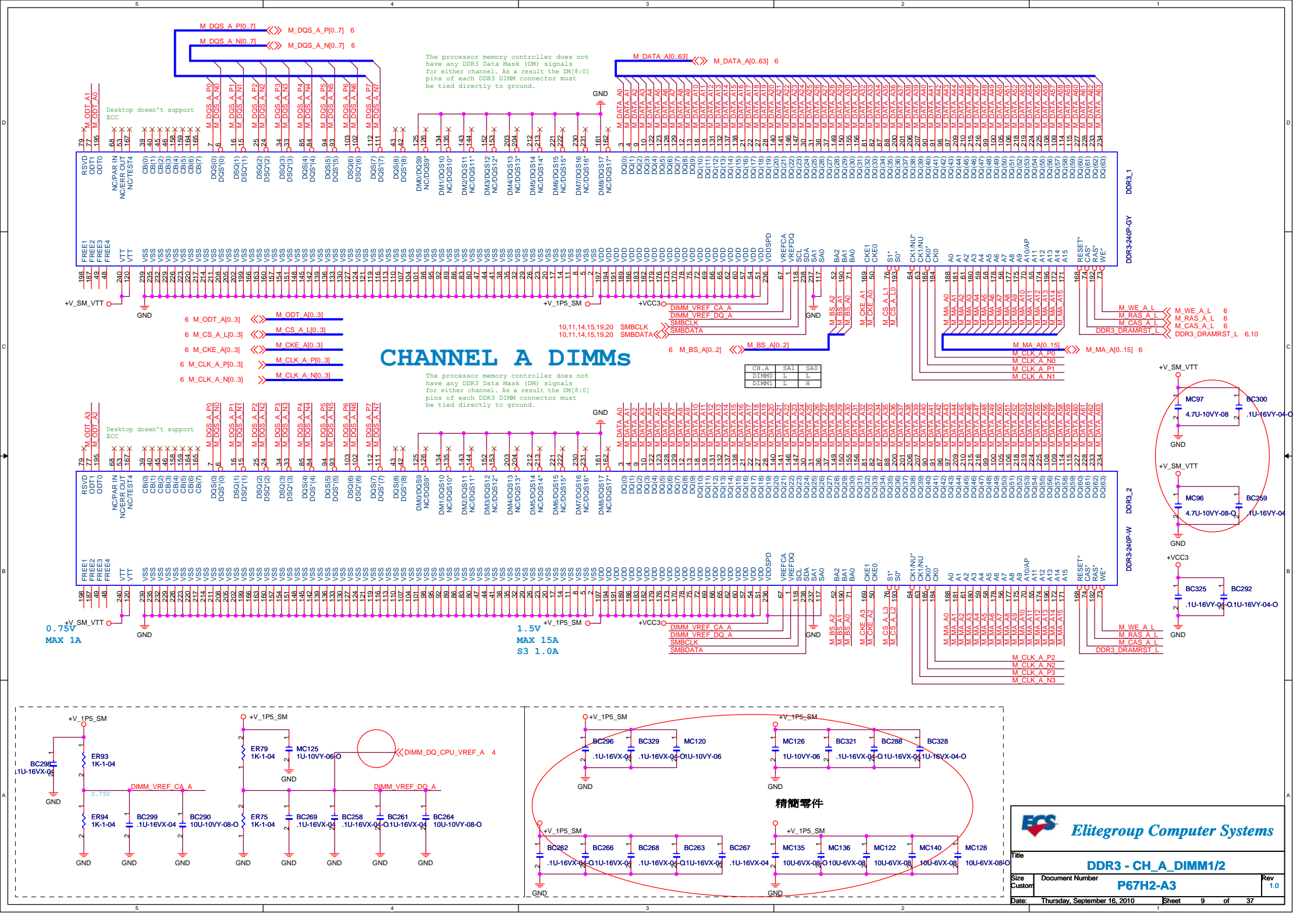


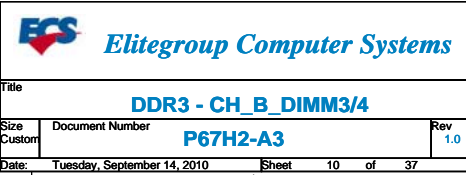
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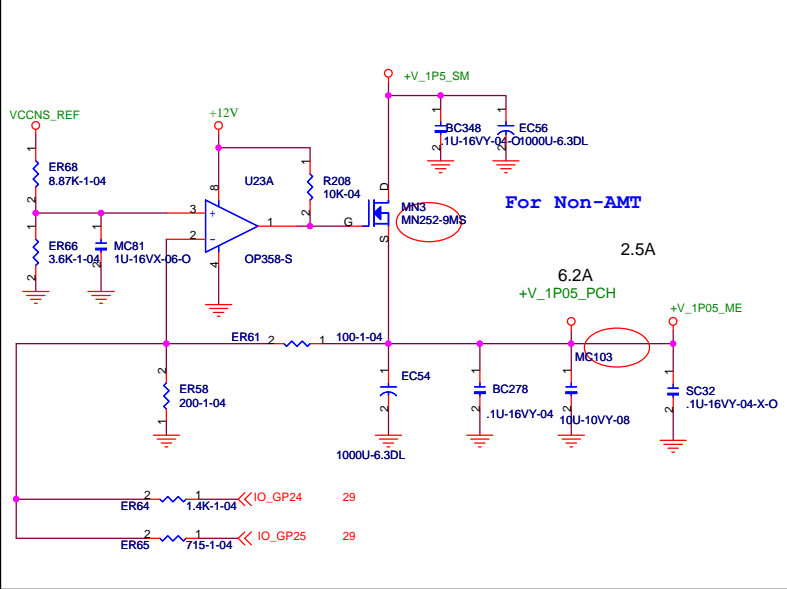
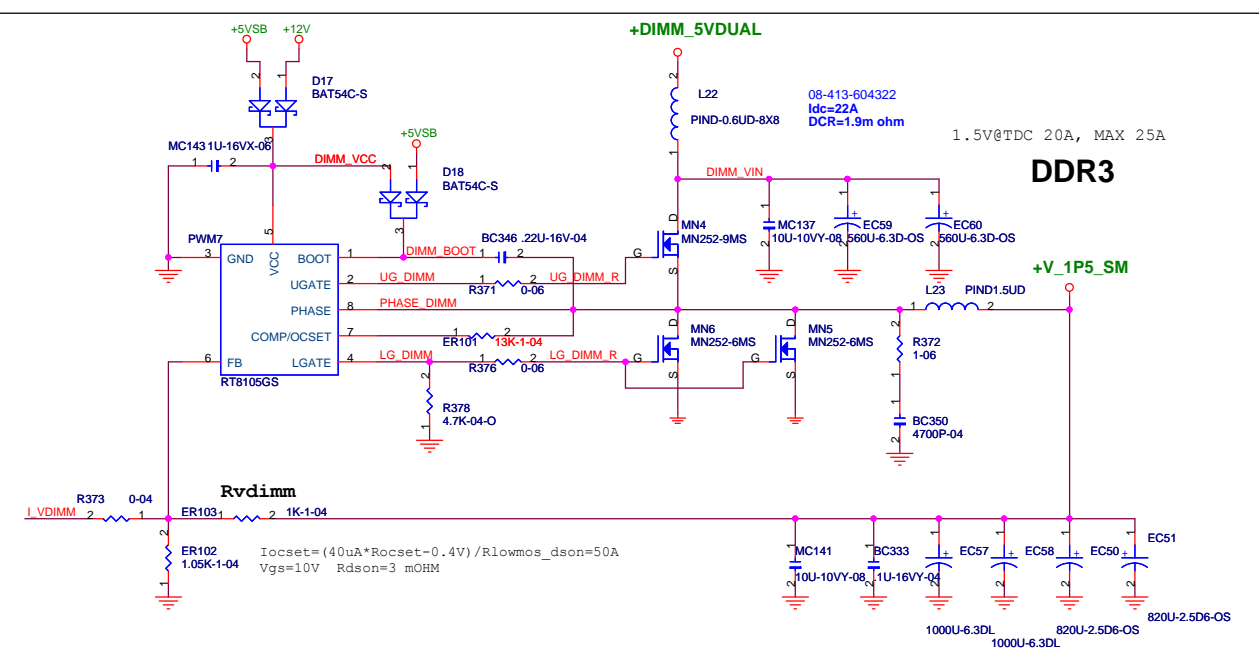
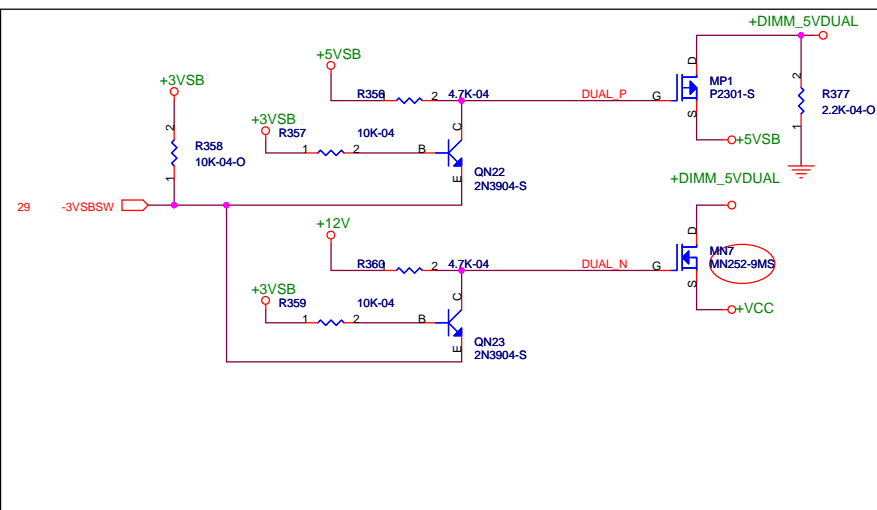


## VCCSA Sequence







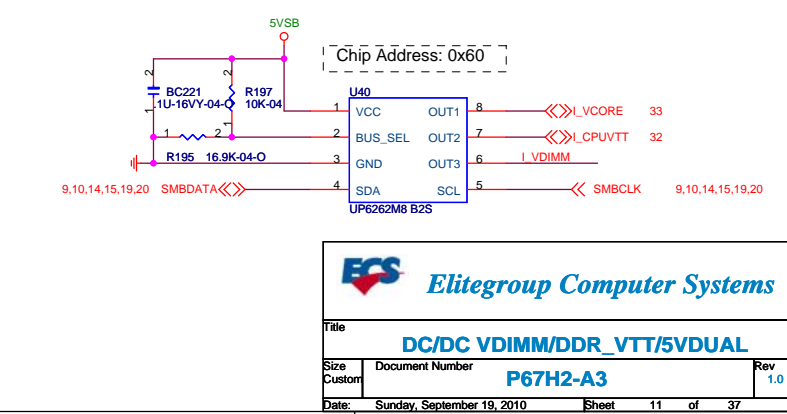
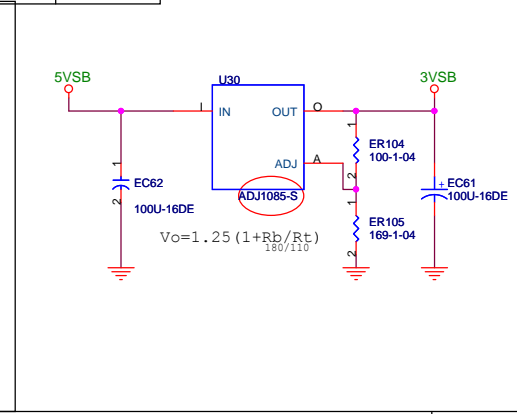
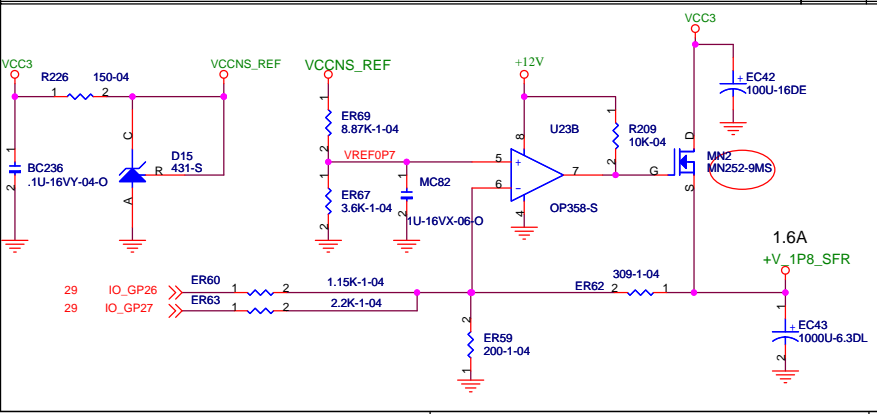
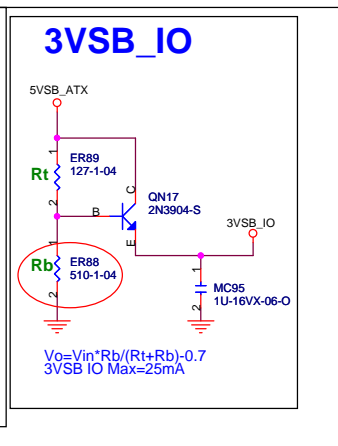
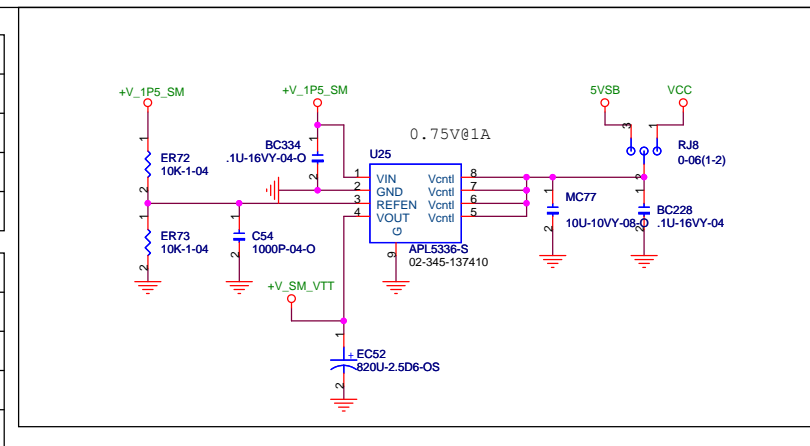


W Monitor :1.05V (Traget)


GP24	GP25	PCH
1	1	1.08V
0	1	1.13V
1	0	1.18V
0	0	1.23V

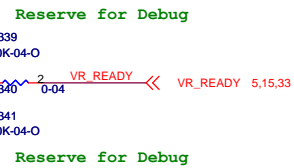
W Monitor :1.8V (Traget)

GP26	GP27	PLL
1	1	1.83V
0	1	1.93V
1	0	2.02V
0	0	2.13V

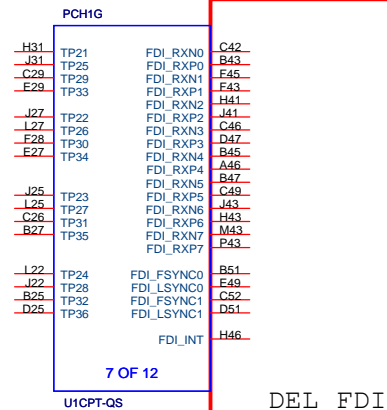


Date: Thursday, September 16, 2010 Sheet 12 of 37

 <b>Elitegroup Computer Systems</b>			
Title			
<b>PCH - SATA, SATA CONN</b>			
Size Custom	Document Number		Rev
	<b>P67H2-A3</b>		<b>1.0</b>
Date:	Monday, September 20, 2010		Sheet 13 of 37







Renamed NV\_WE#[CK[0:1], NV\_RE# WRB[0:1], NV\_RCOMP, NV\_RB#, NV\_DQ9 / NV\_IO[0:15], NV\_DQS[0:1], NV\_CE#[0:3], and NV\_ALE to Reserved(RSVD).  
Renamed NV\_CLE to DF\_TVS.



ME\_UNLOCK

1  
2

H2X1-B

ME\_UN\_PU

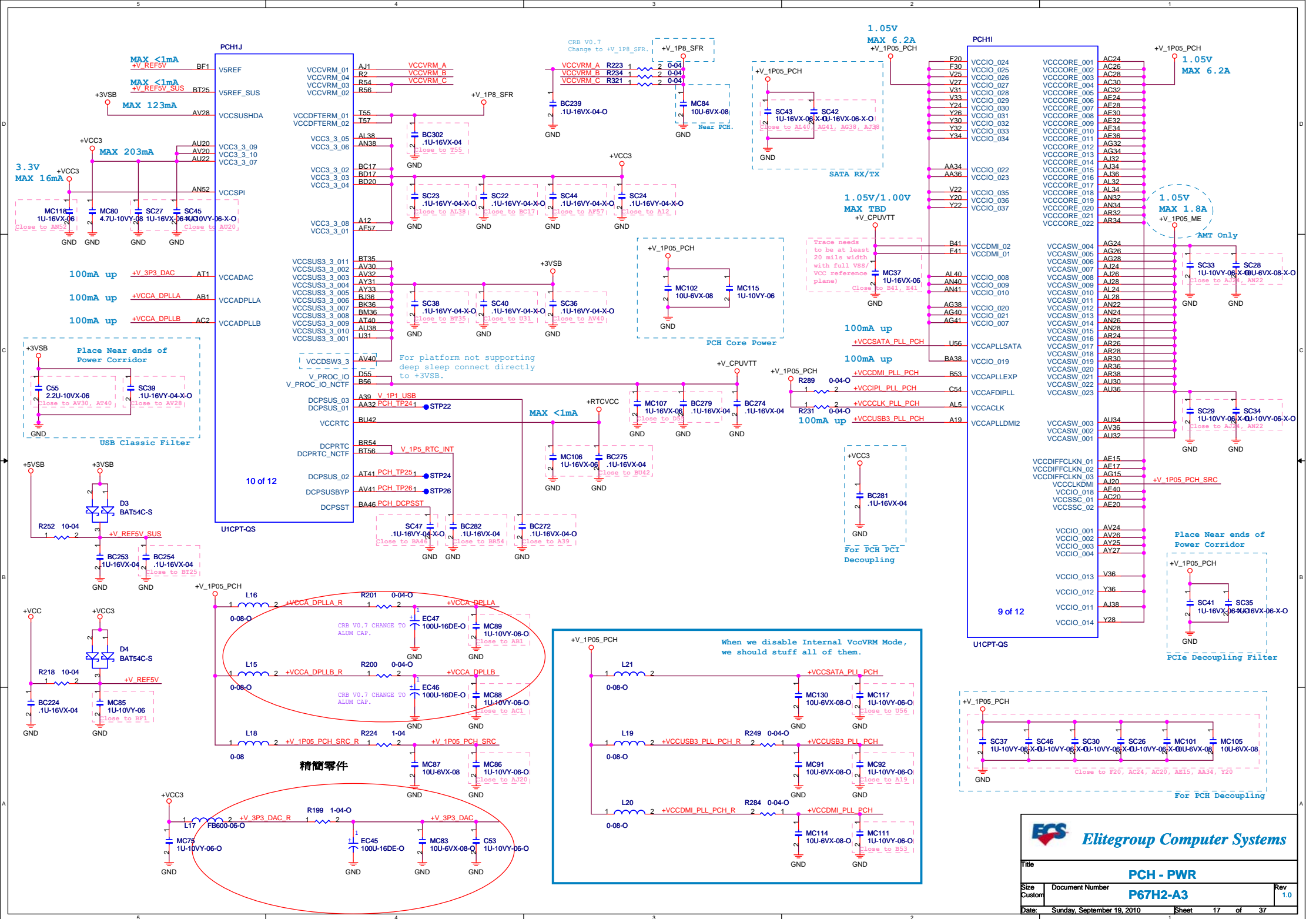
HDA\_SDOUT\_R

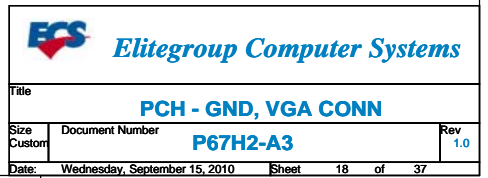
HDA\_SDOUT\_R 1

3V3SB

R287  
1K-04

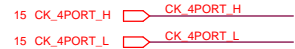
	ME_UNLOCK
1-2	UNLOCK
Float	LOCK





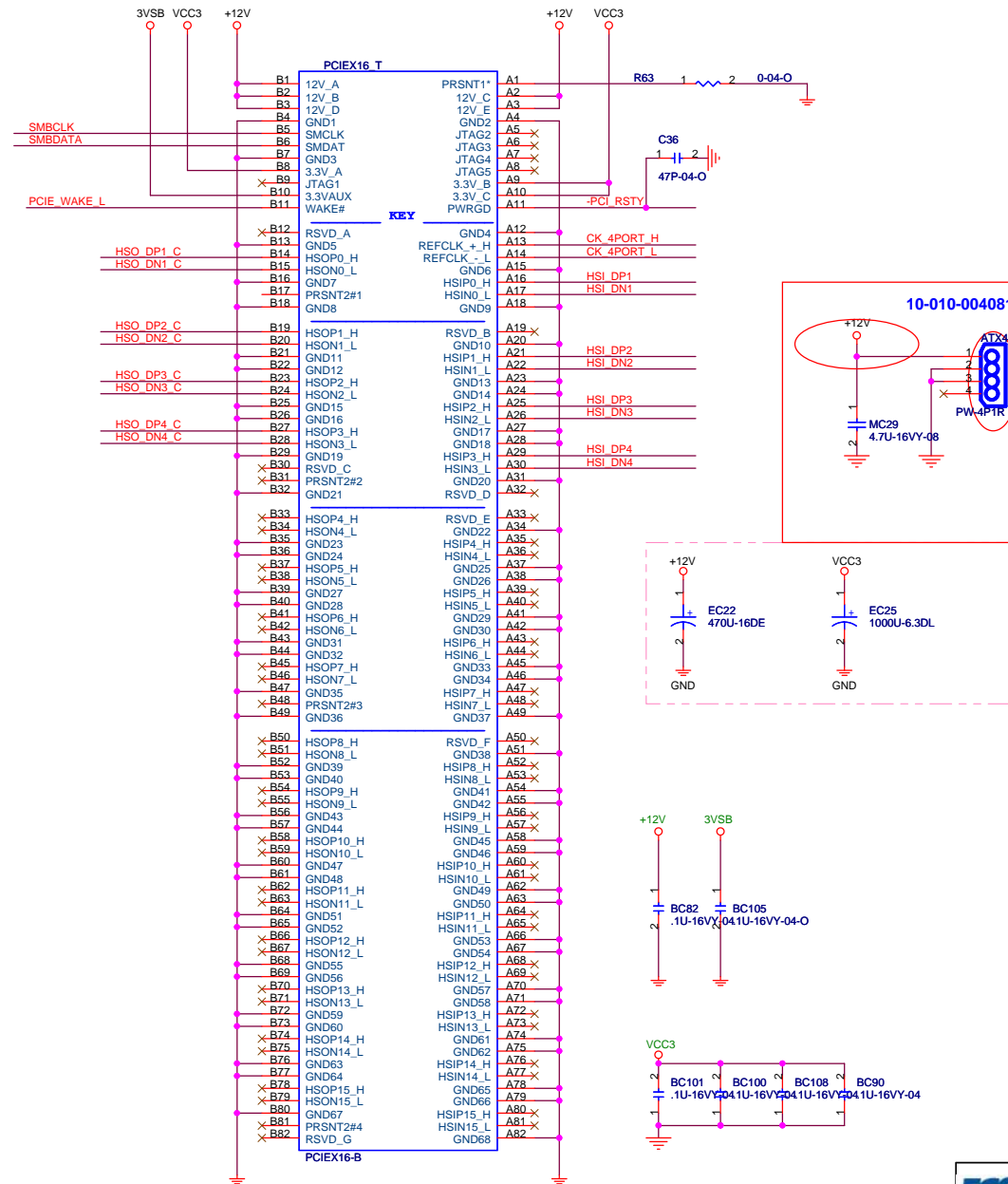



## External Connection



HSO DN1	C37	1	21U-16VX-04	HSO DN1 C
HSO DP1	C38	1	21U-16VX-04	HSO DP1 C
HSO DN2	C41	1	21U-16VX-04	HSO DN2 C
HSO DP2	C40	1	21U-16VX-04	HSO DP2 C
HSO DN3	C43	1	21U-16VX-04	HSO DN3 C
HSO DP3	C42	1	21U-16VX-04	HSO DP3 C
HSO DN4	C45	1	21U-16VX-04	HSO DN4 C
HSO DP4	C44	1	21U-16VX-04	HSO DP4 C

Near chipset



**Elitegroup Computer Systems**

Title

Slot - PCI-EX16-2

Size Custom

Document Number

P67H2-A3

Rev 1.0

Date: Friday, September 17, 2010

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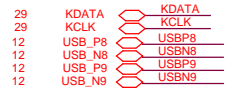
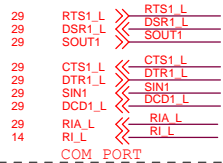


## Debug Card

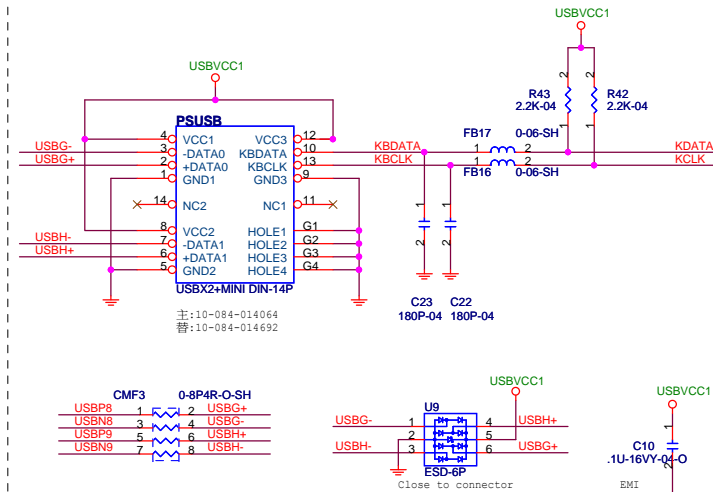
```
del debug card
```

```
del debug card
```

## Debug Card

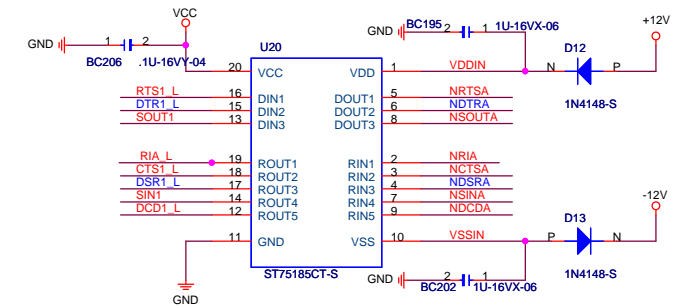
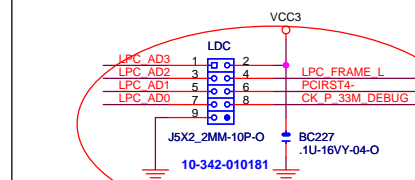


PS2/USB

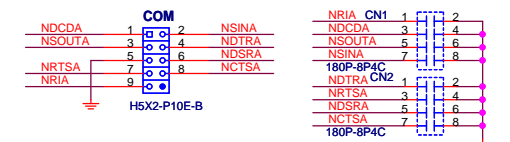


## PS2/USB Header Circuit

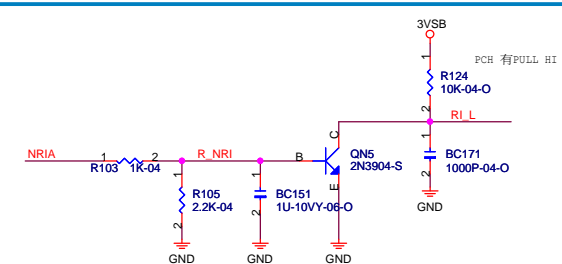
## LPC DEBUG HEADER



	<b>NR1A</b>	<b>RI#</b>
<i>Normal</i>	-12V	<i>High</i>
<i>Active</i>	+12V	<i>Low</i>

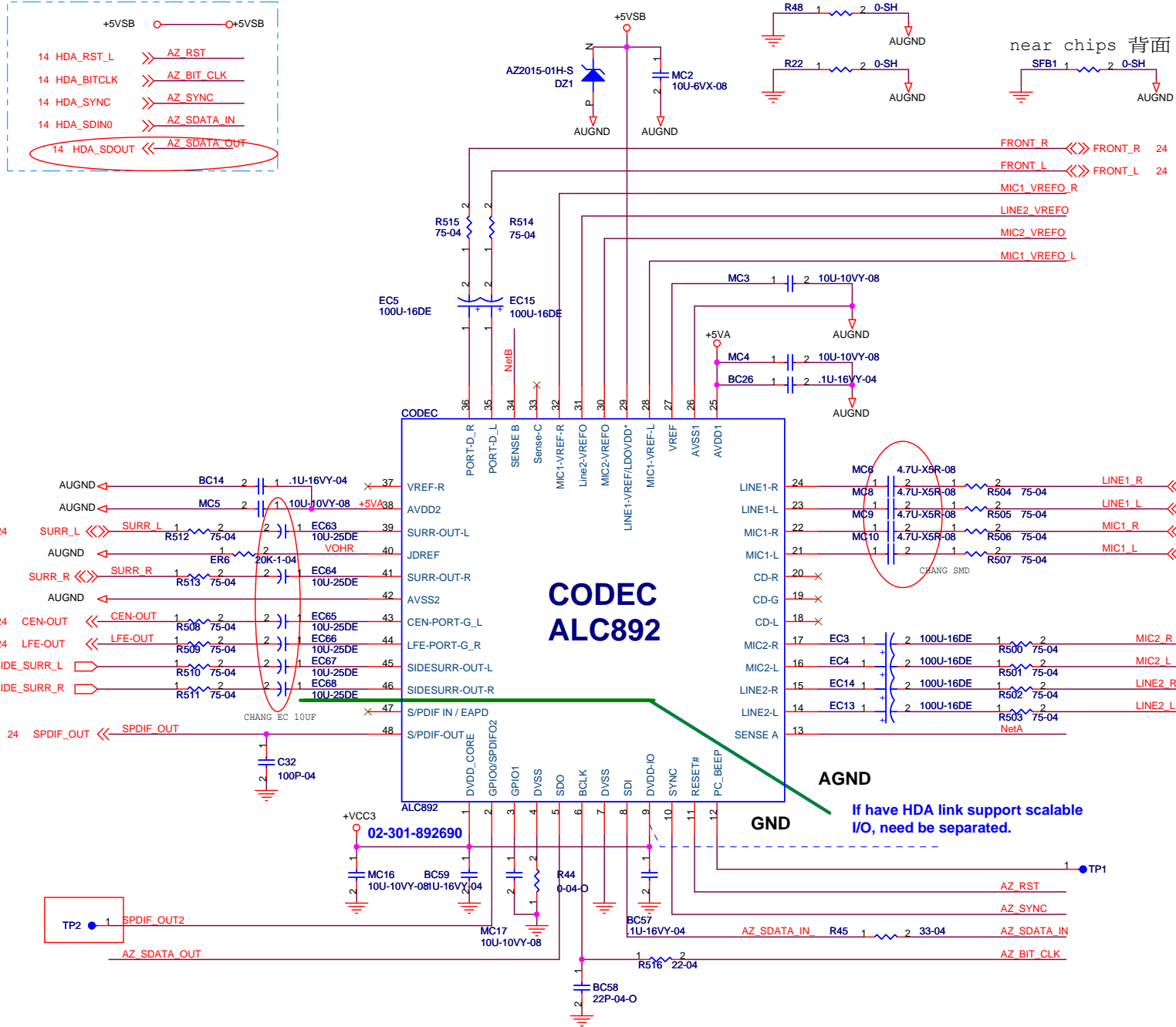
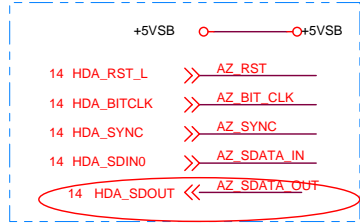


### COM Header Circuit

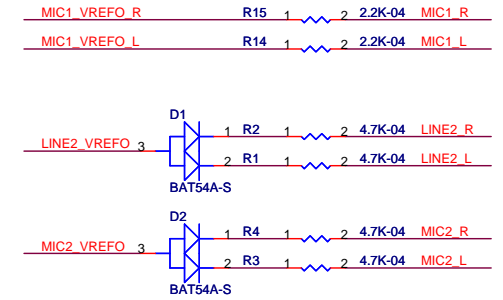


## COM RI# Wake Up Circuit

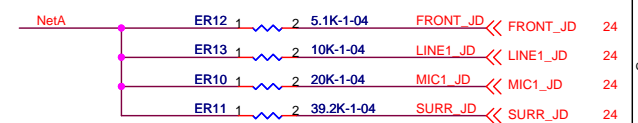
## External Connection



## Verfourt bias for stereo microphone.



## Place near codec Resistors Networks



**Elitegroup Computer Systems**

**Audio - ALC892**

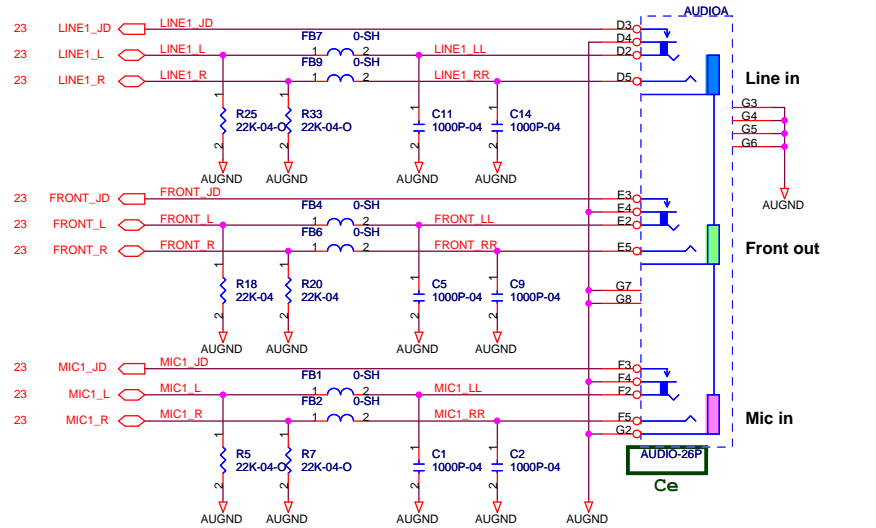
**P67H2-A3**

**Rev 1.0**

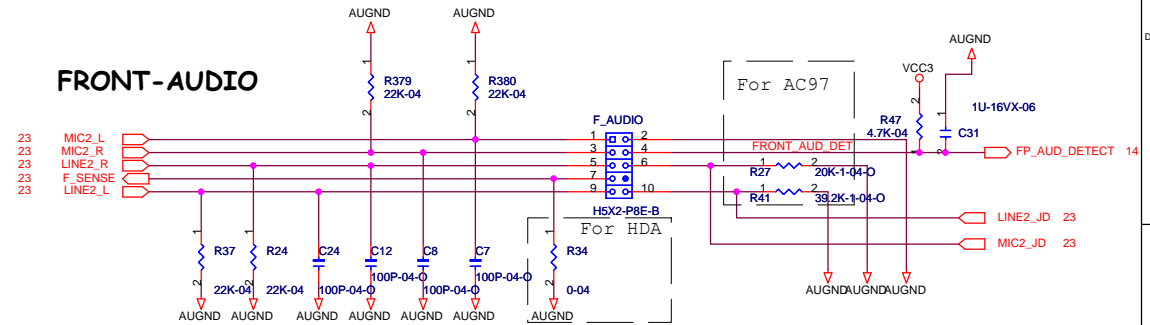
**Date: Friday, September 17, 2010**

**Sheet 23 of 37**

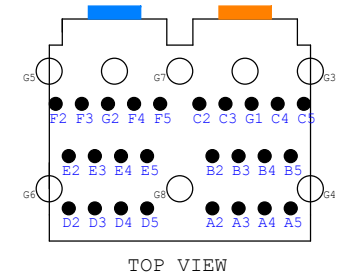
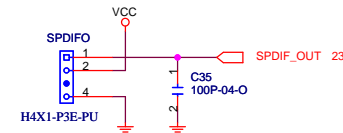
## REAR-AUDIO



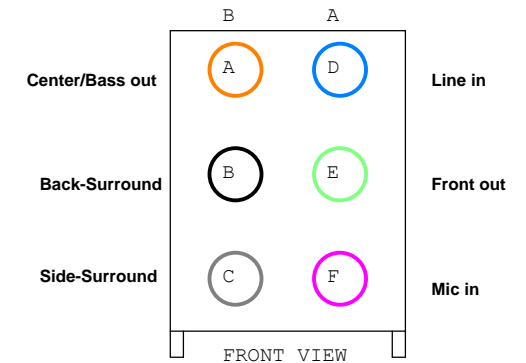
## FRONT-AUDIO



## SPDIF-OUT



TOP VIEW



FRONT VIEW



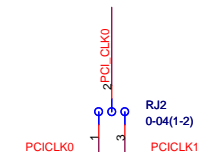
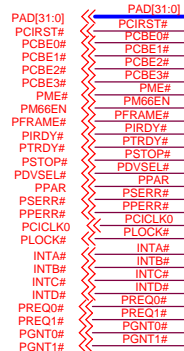


# External Connection

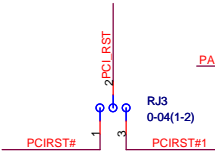


15 PCICLK\_EXT << PCICLK1  
2 PCILPCAID\_RST\_L << PCIRST#1

## COMMON

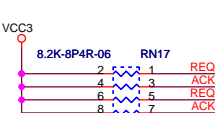
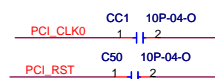
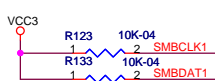


1-2: Internal PCICLK  
2-3: External PCICLK



1-2: Internal PCIRST  
2-3: External PCIRST

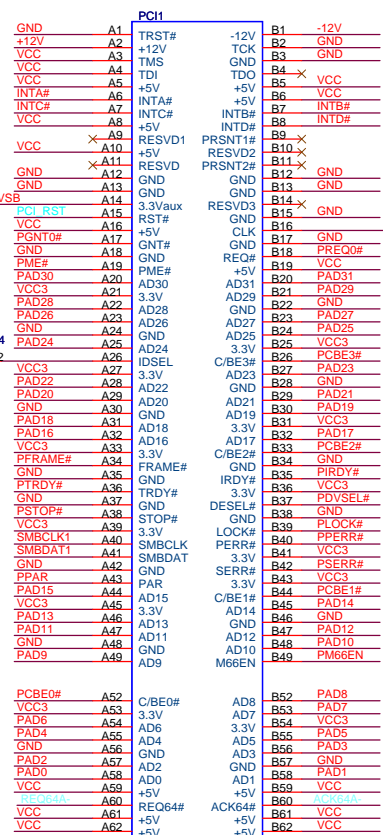
## PCI CHIP



0406 gavin

PCI1:REQ0;GNT0 IDSEL:16 INT:ABCD  
PCI2:REQ1;GNT1 IDSEL:17 INT:BCDA

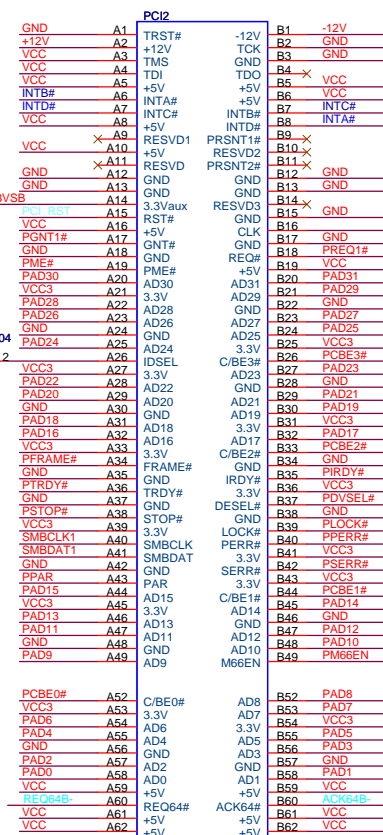
## PCI1



## PCI-W



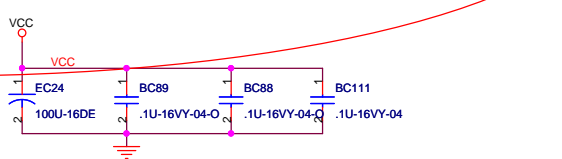
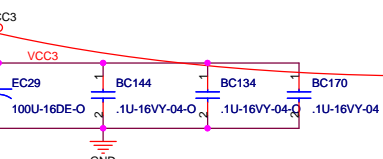
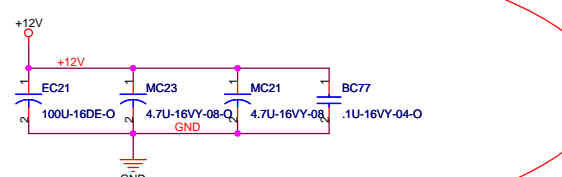
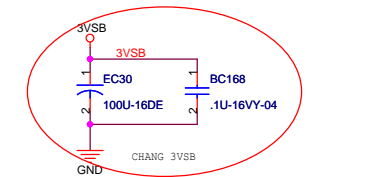
## PCI2



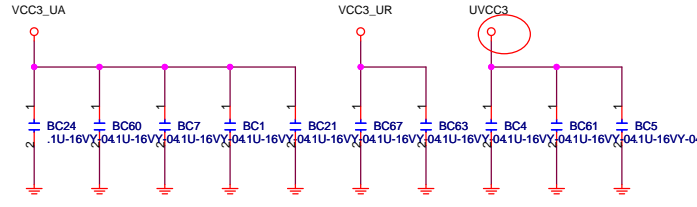
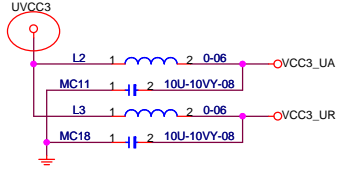
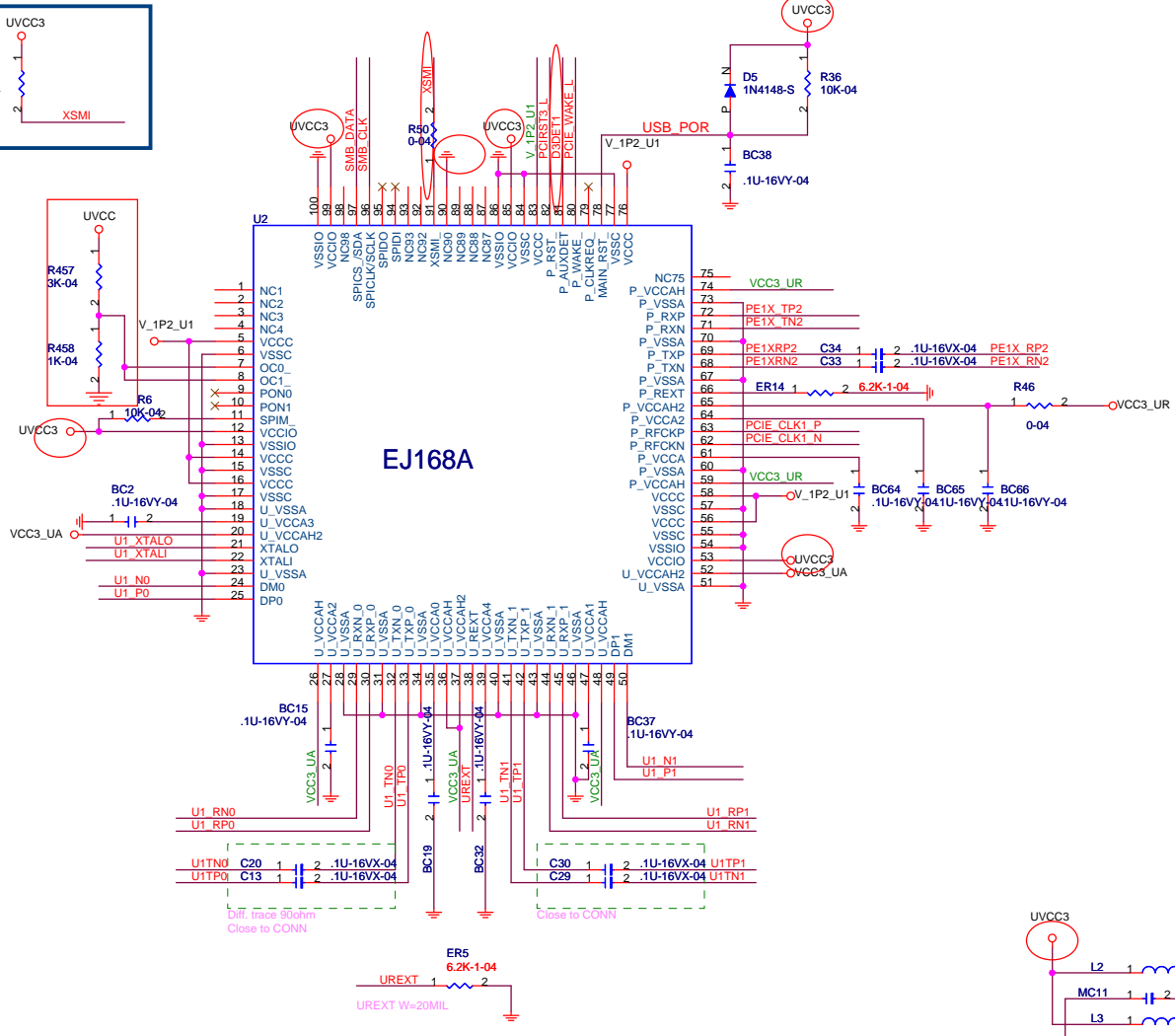
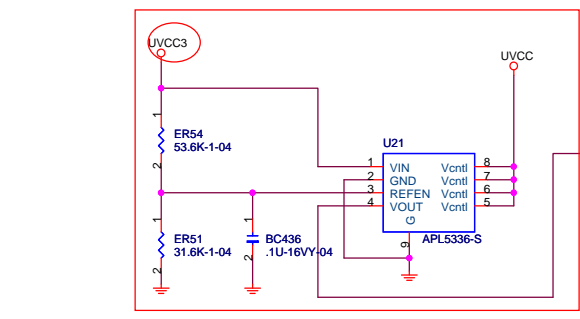
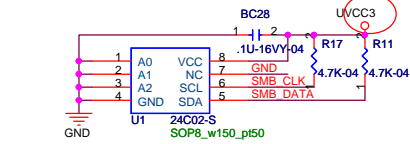
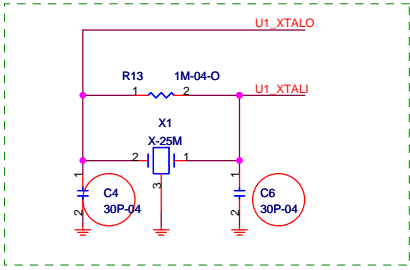
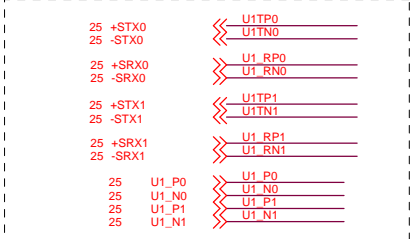
## PCI-W



## 精簡零件



22,25,29	SIO_PCIRST3_L	>>>	PCIRST3_L
14,19,20,25,26	PCIE_WAKE_L	>>>	PCIE_WAKE_L
15	CK_PE_USB3_H	>>>	PCIE_CLK1_P
15	CK_PE_USB3_L	>>>	PCIE_CLK1_N
12	USB3_TX_P3	>>>	PE1X_TP2
12	USB3_TX_N3	>>>	PE1X_TN2
12	USB3_RX_P3	>>>	PE1X_RP2
12	USB3_RX_N3	>>>	PE1X_RN2
14	XSMI	>>>	XSMI



	Wake up	No Wake up
U3a	RJ12 (1-2)	RJ12 (2-3)
U3b	R385,R382	R383,R384



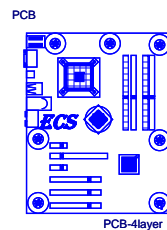
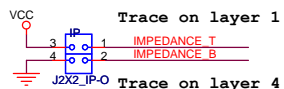
### 1)Circuit type 1

Layer 1:TOP

Layer 2:PWR

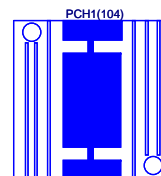
Layer 3:GND

Layer 4:BOTTOM



PCB STACK: L1:TOP  
L2:PWR  
L3:GND  
L4:BOTTOM

20-120-012343



20-120-010851

PN:20-120-010851

CLR\_CMOS(1-2)

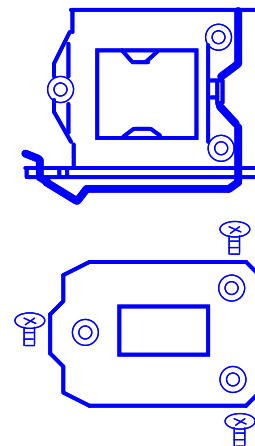


JP-R

11-018-115021 CPU SMD SOCKET  
SOCKET.CPU.LGA.1155P.SMD.BLACK.PE115527-4041-01F.  
LEAD-FREE.FOXCONN

20-800-004711 CPU SOCKET STEEL  
SUBASSY.STEEL.LGA.1156P.W/  
BACK PLATE.PT44A11-6401.LEAD-FREE(RoHS).FOXCONN

CPU1(104)  
CPU\_SUBASSY\_STEEL



01D201-000060 PCH ES0

BT(104)



CR2032

Y1(wire)



JP-WI-P6.25



Elitegroup Computer Systems

Title

Size  
Custom

Document Number

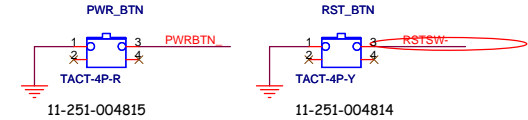
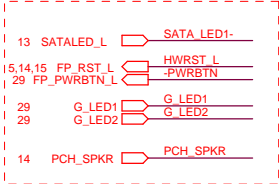
P67H2-A3

Rev  
1.0

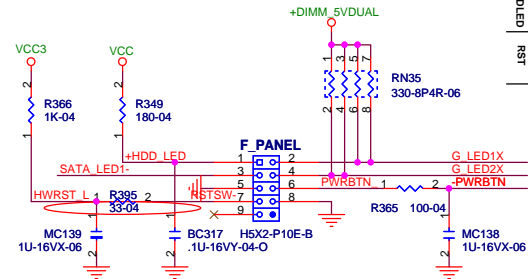
Date: Thursday, September 23, 2010

Sheet 30 of 37

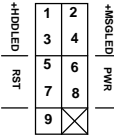
External Connection



FRONT PANEL

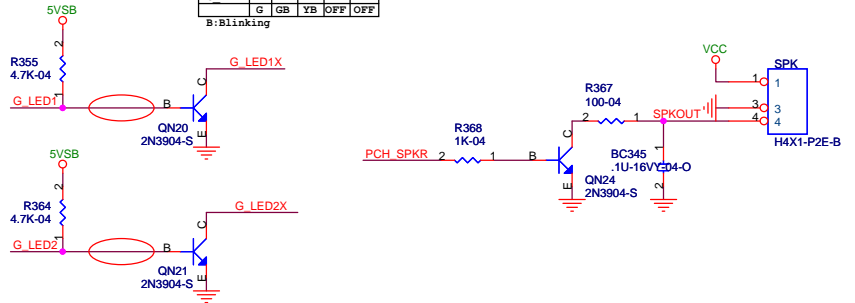


F. PANEL



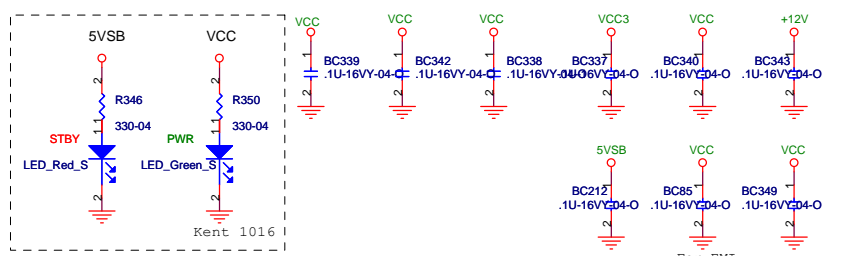
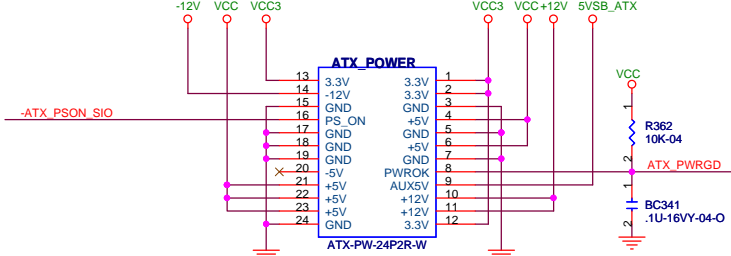
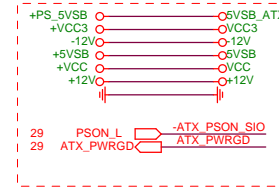
	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
G	GB	YB	OFF	OFF	OFF

B: Blinking



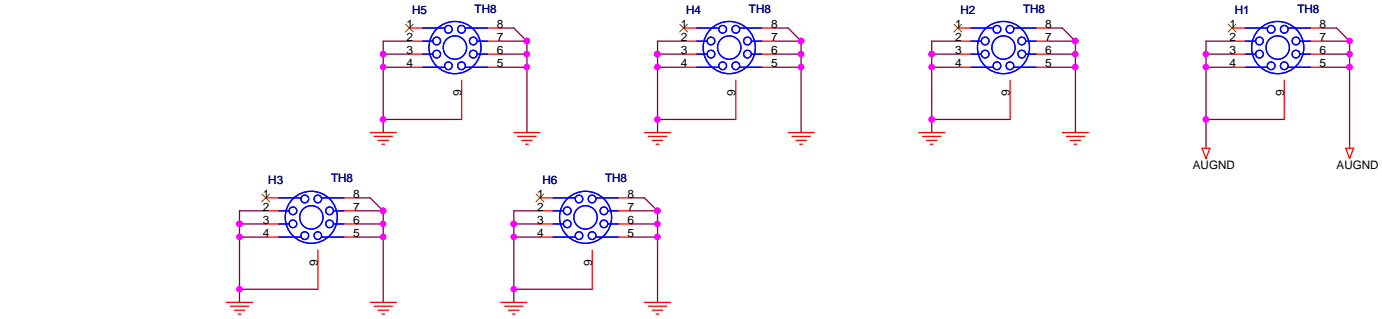
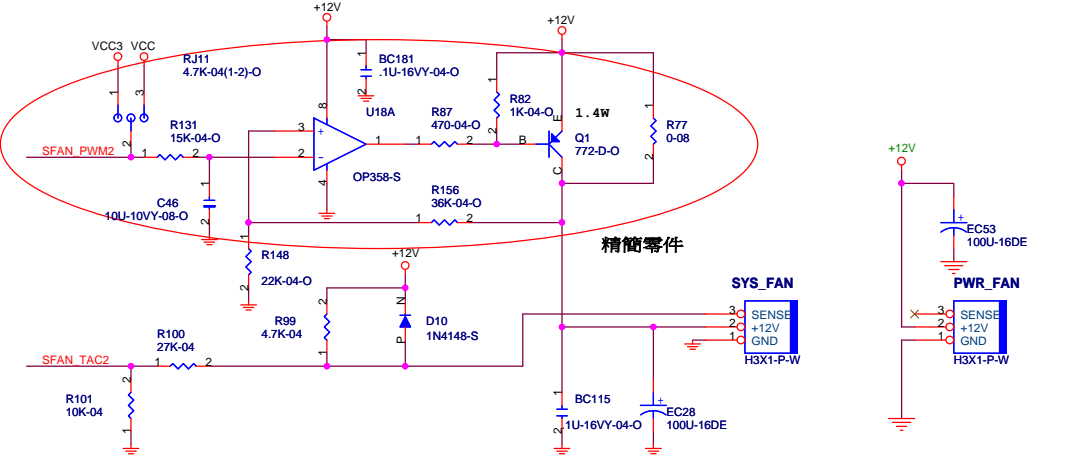
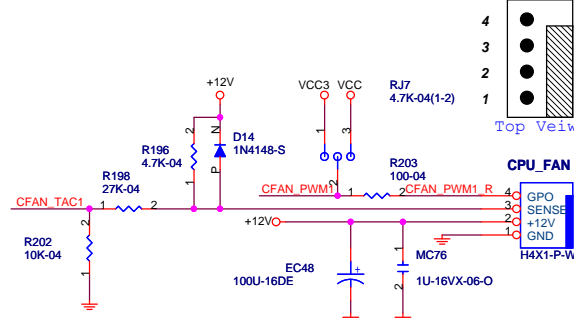
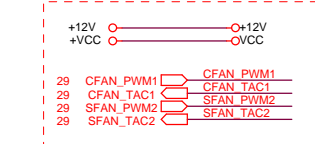
POWER CONNECTOR

External Connection

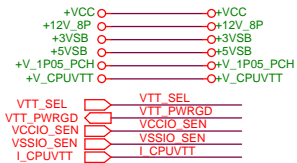


FAN

External Connection

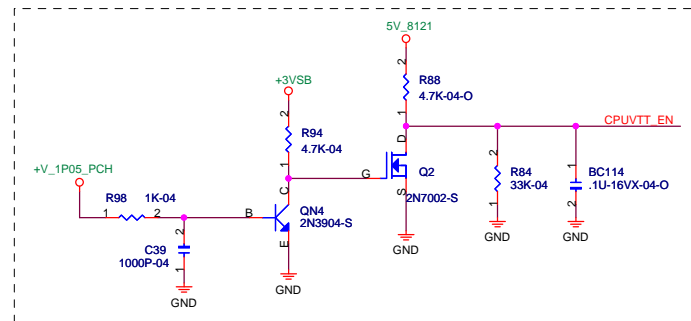
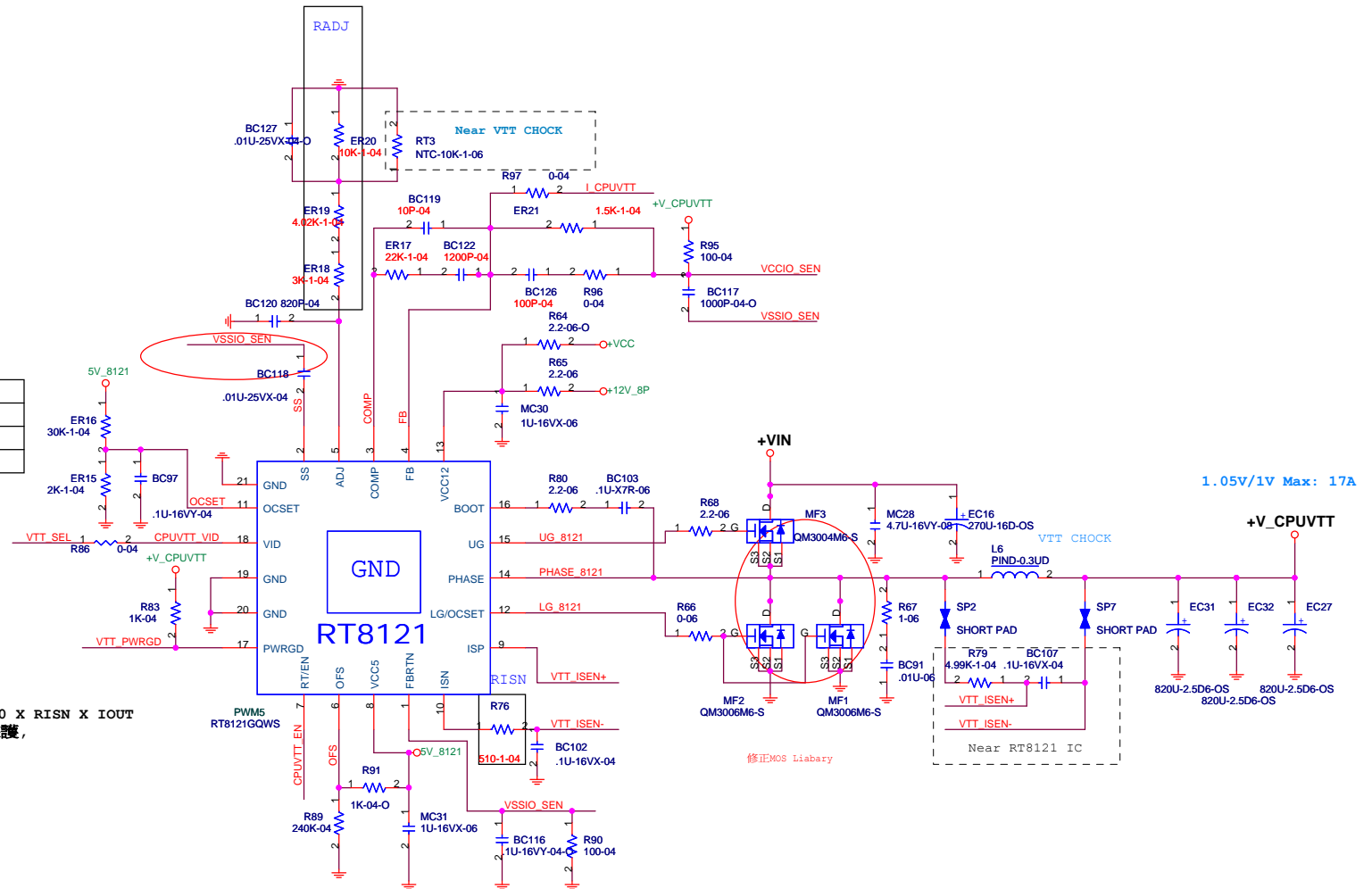


## External Connection

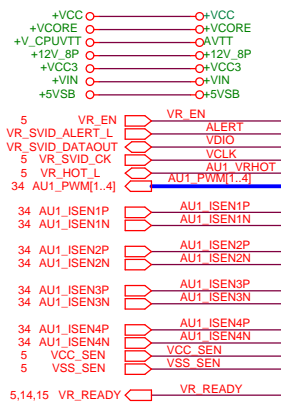


VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V

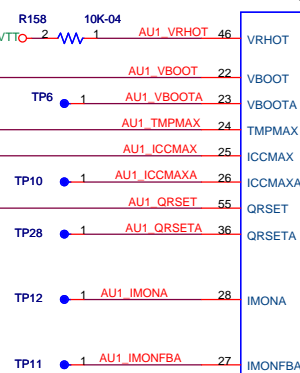
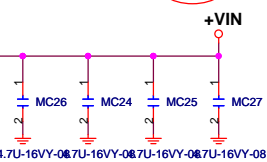
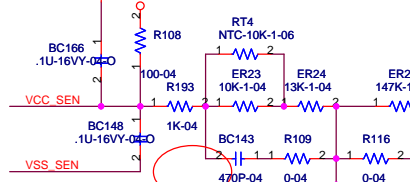
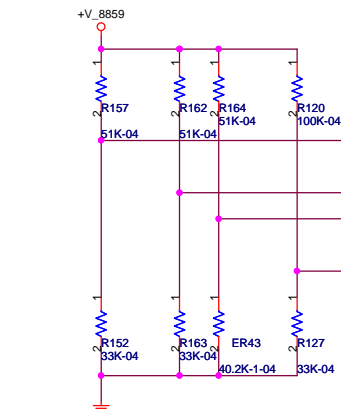
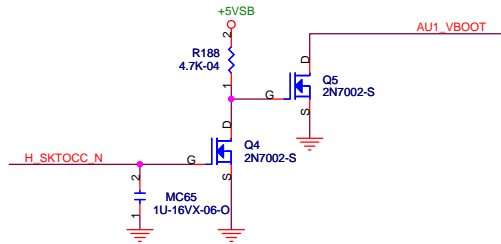
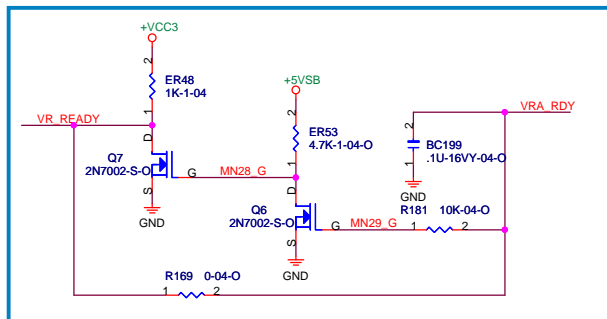
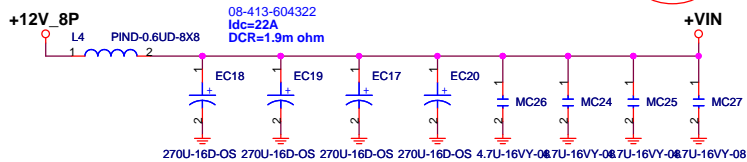
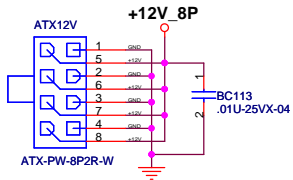
$VADJ = LL \times IOUT = DCR \times RADJ / 20 \times RISN \times IOUT$   
 OCP設定方式就是VADJ > VOCSET 時保護，



## External Connection

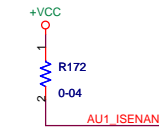
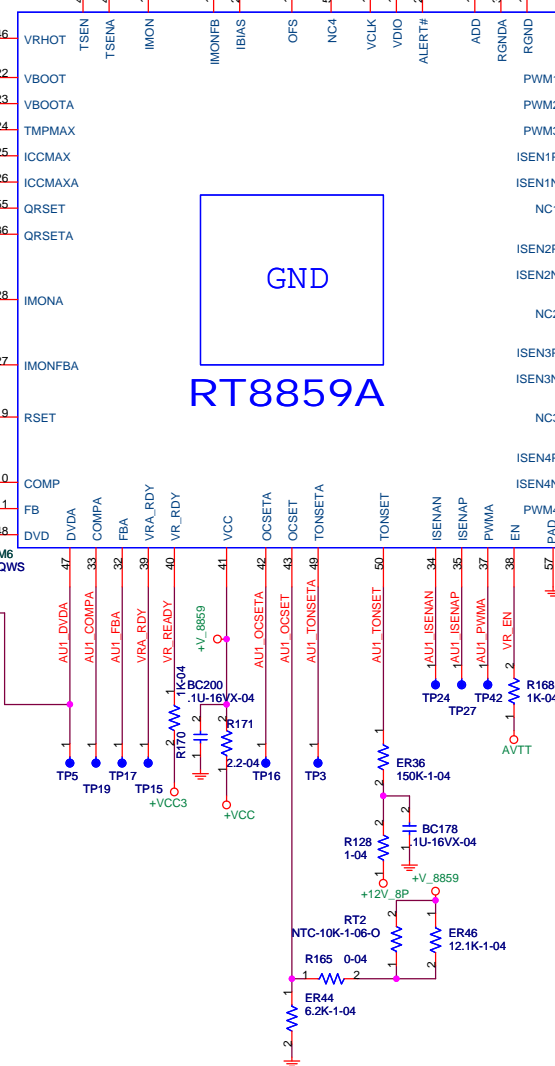


DEL VAXG



GND

**RT8859A**

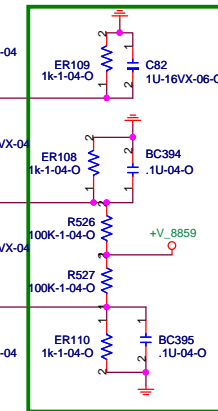


## BOM Difference

	RT8859A	RT8859M
Ca	X	V
Cb	X	V
Cc	X	V
Cd	402-1-04	1k-1-04



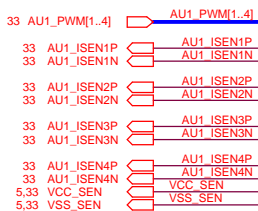
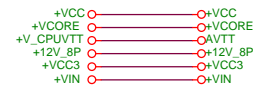
**Cb**



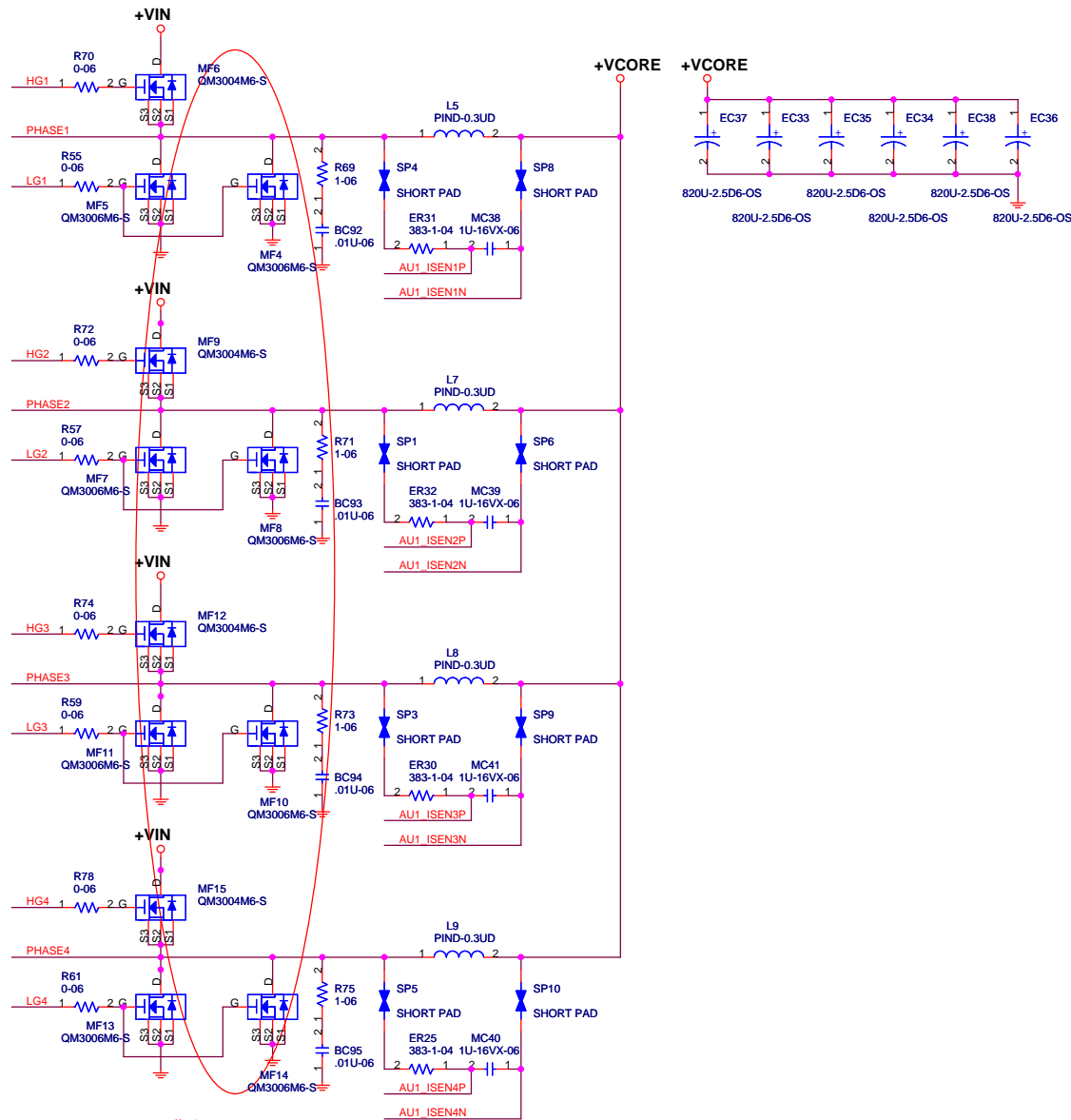
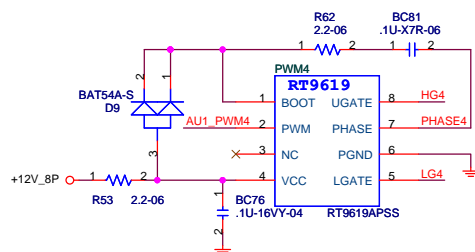
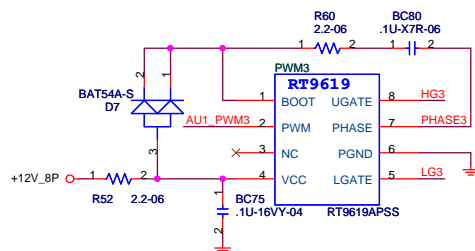
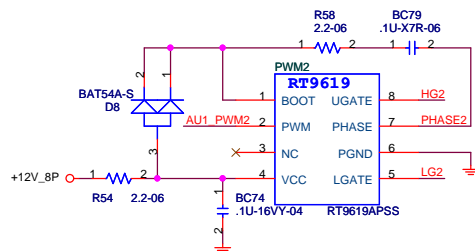
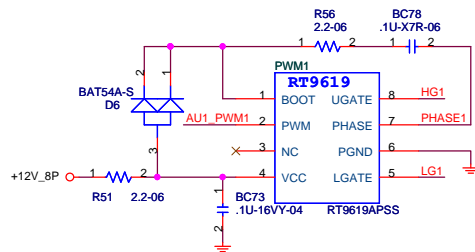
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Custom			
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## External Connection



DEL VAXG



DEL VAXG

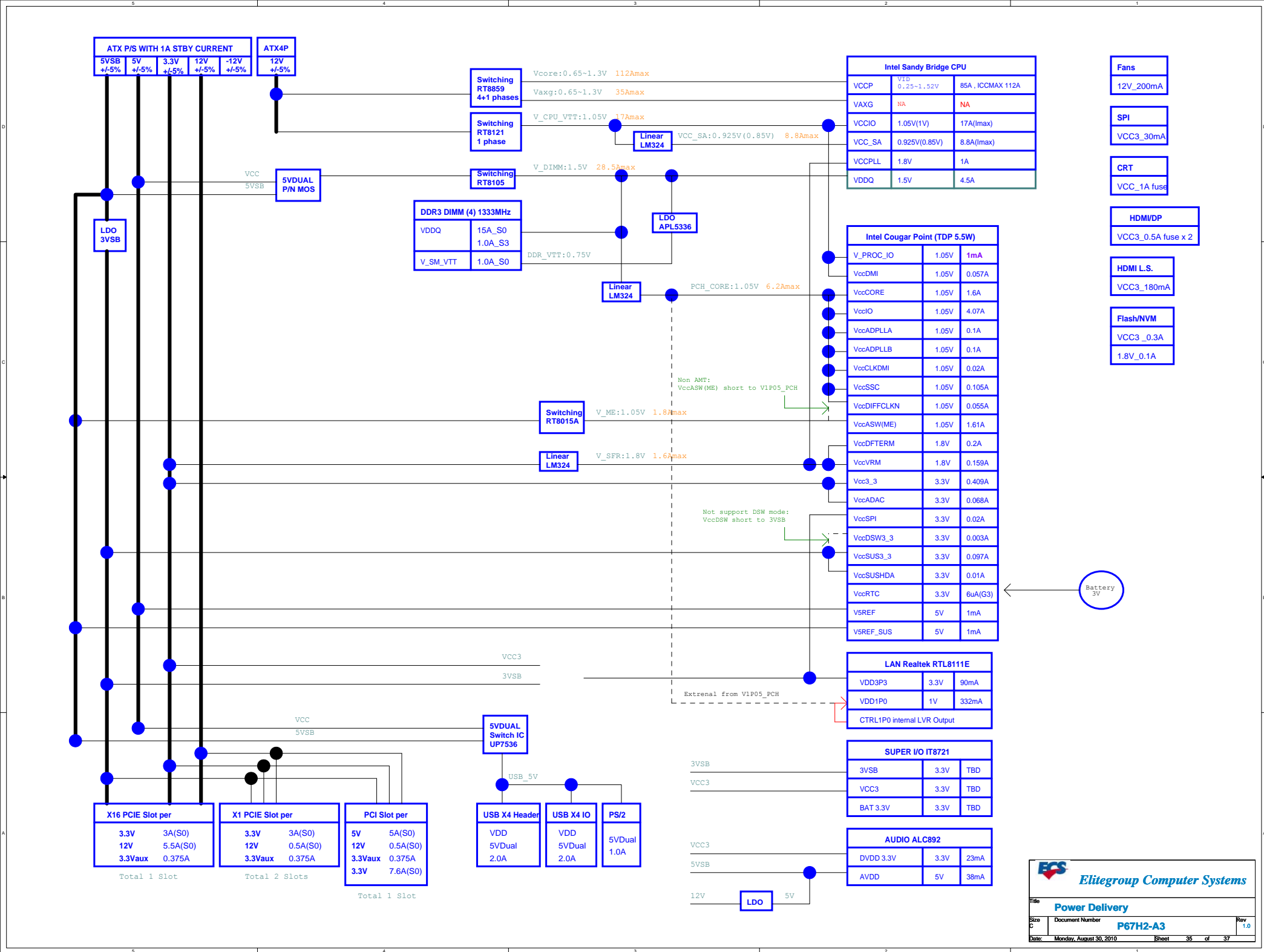


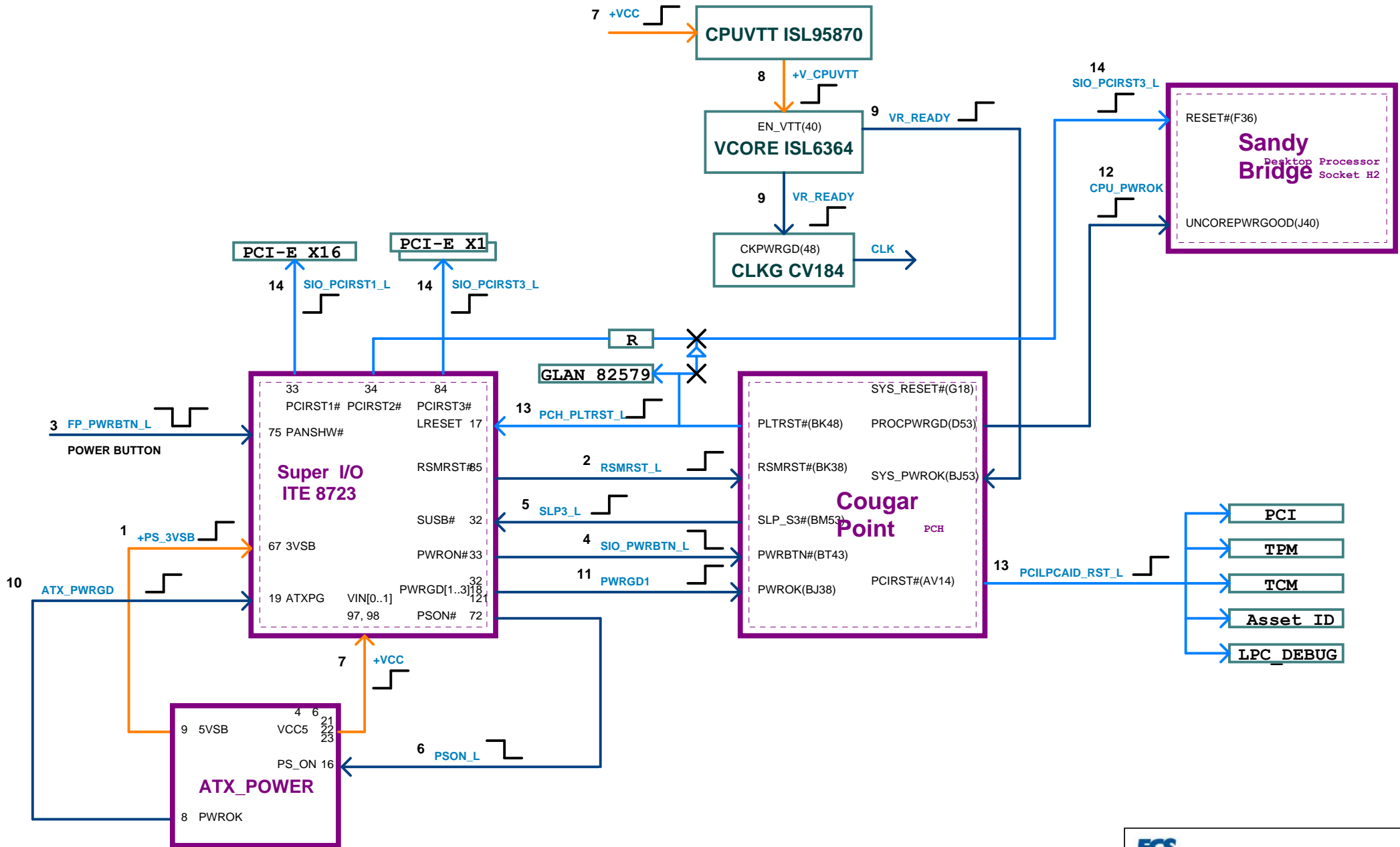
Elitegroup Computer Systems

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**NOTE:**

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

